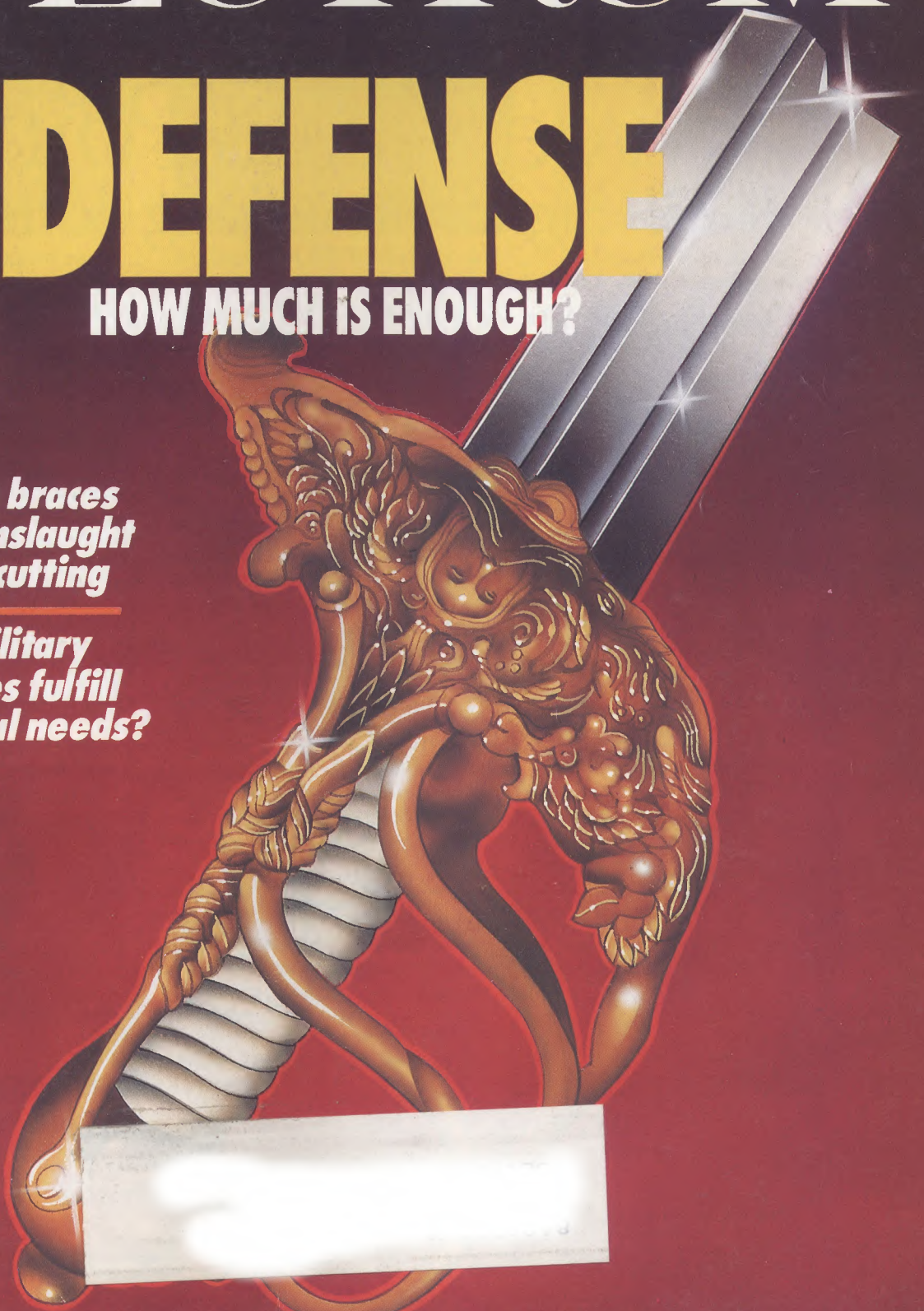
SPECIAL **SOFTWARE** GUIDE, P.45

IEEE

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DEFENSE

HOW MUCH IS ENOUGH?

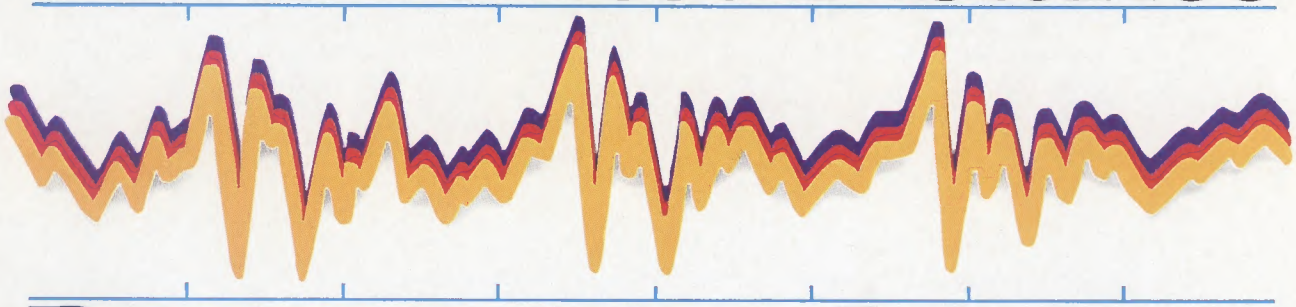


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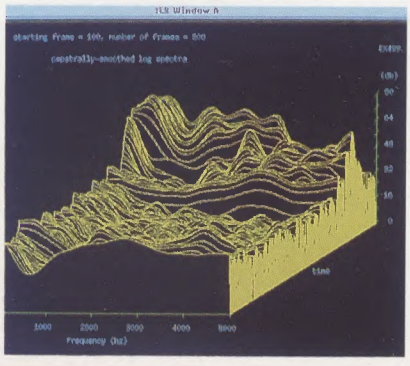
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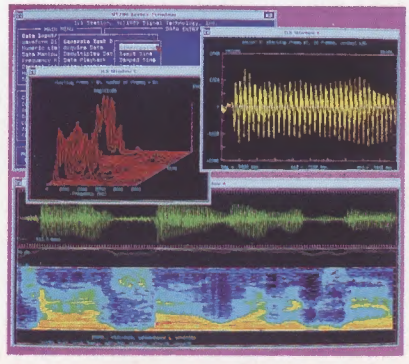


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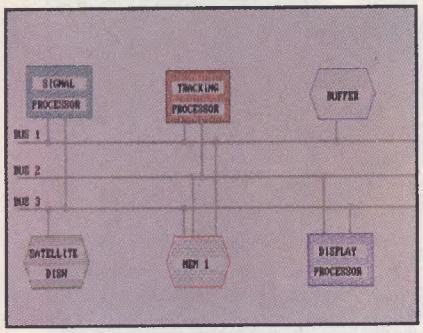
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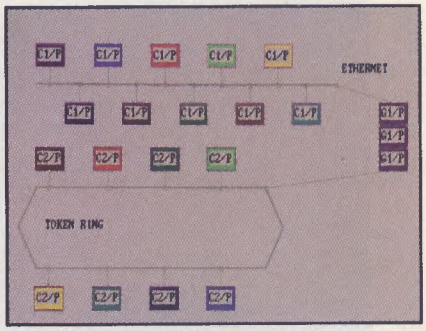
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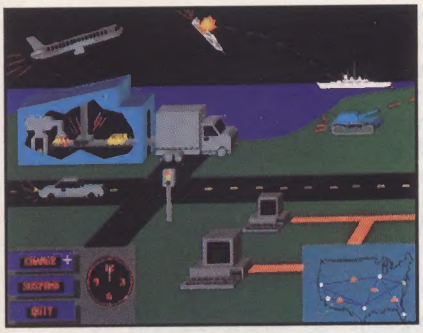
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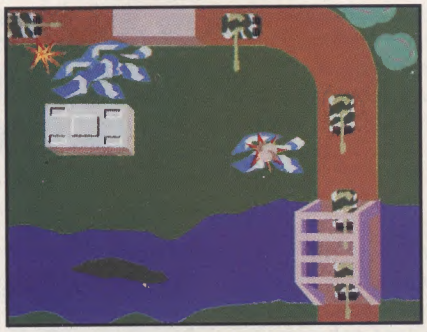
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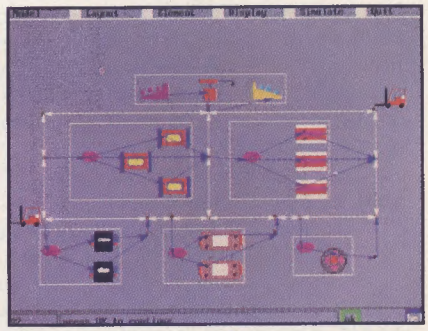
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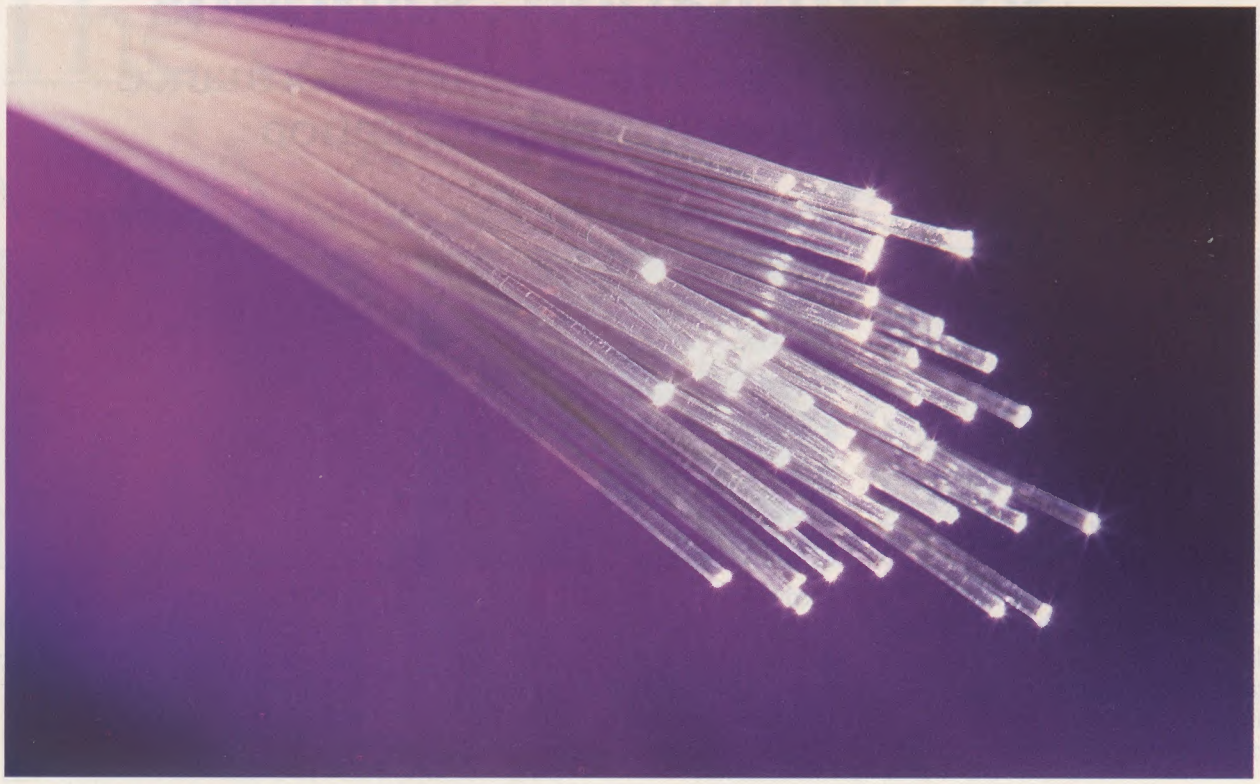
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NEWSLOG

SEP 6: **The U.S. National Space Council** announced a new space policy requiring satellites owned by the U.S. government—like military satellites or scientific missions operated by NASA—to be launched only on U.S. produced rockets.

SEP 6: Two **Los Angeles** utilities, the **Department of Water and Power** and the **Southern California Edison Co.**, said they would develop a mass-producible electric four-passenger car and put 1000 of them on the city's streets by late 1992. **Clear Air Transport**, a company in Göteborg, Sweden, will design the car, which will have a range of 250 kilometers between charges, travel at a top speed of 110 kilometers per hour, and initially cost US $25 000.

SEP 11: In the first big test of the **Semiconductor Chip Protection Act of 1984**, a Federal district court jury in San Diego, Calif., found that **Advanced Micro Devices Inc.**, Sunnyvale, Calif., had violated three chip patents of **Brooktree Corp.**, San Diego, and infringed on Brooktree's rights to protect chip layout designs under the 1984 law. Advanced Micro said it would appeal.

SEP 12: **GTE Airfone**, a cellular telephone service in Oak Brook, Ill., and **Communications Satellite Corp.**, Washington, D.C., said they would make the first global airline phone service available in mid-1991.

SEP 13: A Federal panel, led by Lew Allen, director of NASA's Jet Propulsion Laboratory, said a design defect in a metering rod—a measuring device that was used to set up the **Hubble Space Telescope's** main mirror—probably compounded by human error during assembly, caused the mirror flaw in the instrument. Allen said there was strong evidence that the metering rod was installed upside down.

SEP 14: **Telefónica de España SA** of Spain agreed to take a 6 percent stake in AT&T Co.'s main European holding company, based in the Netherlands, in exchange for its 20 percent share in a Spanish chip company, **AT&T Microelectrónica SA**. The holding company, **AT&T Network Systems International BV**, now owns 100 percent of AT&T Microelectrónica, which in 1985 built a US $200 million custom chip factory near Madrid.

SEP 15: Eight of Silicon Valley's smaller chip-makers have joined to fight patent-infringement claims brought by larger rivals, some of which they contend use patent and copyright litigation less as a protective measure than as a revenue-generating tool. The chip-makers are **Cypress Semiconductor, Integrated Device Technology, LSI Logic, VLSI Technology, Altera, Sierra Semiconductor, Linear Technology,** and **Seeq Technology**.

SEP 17: **IBM Corp.** and **Microsoft Corp.**, Redmond, Wash., whose alliance has dominated the workstation world, redefined how they will work together in developing PC software: IBM will develop new versions of OS/2 for use on computers running on Intel Corp.'s 80286 and 80386 processors, and Microsoft will develop a portable version of OS/2 that will run on microprocessors other than Intel's—mainly chips that use reduced-instruction-set computing technology.

SEP 19: **IBM Corp., MCI Communications Corp.**, Washington, D.C., and **Merit Inc.**, Ann Arbor, Mich., announced formation of a company to manage and expand the Federally financed National Science Foundation Network, enabling it to reach more researchers at universities, Federal laboratories, and corporations.

SEP 19: Signaling a fundamental shift in the economic philosophy of U.S. regulation, the **Federal Communications Commission** gave the eight big U.S. providers of local telephone service—**GTE Corp. and the seven regional Bell companies**—greater freedom starting Jan. 1 to raise or lower the prices they charge long-distance carriers for completing interstate calls, while eliminating most controls on their rate of return.

SEP 20: Tokyo's **NEC Corp.** said it would participate in two Chinese joint ventures to produce digital electronic switching systems and large-scale ICs. The ventures, the first of their kind involving a Japanese electronics company, will significantly advance China's computer and telecommunications industries.

SEP 24: **LSI Logic Corp.**, Milpitas, Calif., introduced a set of chips that the company said would drastically reduce the cost of video conferencing—a large growth market for this decade. Called the L64700 family, the chips will help bring the cost of a typical teleconferencing system down from about US $50 000 today to US $5000 in 1992.

SEP 29: A Soviet environmental official said an explosion at a **nuclear-fuel-processing plant in Kazakhstan** on Sept. 12 may have contaminated 120 000 people. The explosion released toxic beryllium oxide gas, which could lead to lung, eye, and skin problems.

OCT 1: **Advanced Micro Devices Inc.**, Sunnyvale, Calif., introduced a chip that incorporates almost all the components of the circuit board used in the original PC-AT personal computer. It is the first of several announcements expected to come from superchip manufacturers in coming months.

OCT 4: Italy's **Fiat SpA** and France's **Compagnie Générale d'Electricité** (CGE) said they would form a far-reaching strategic alliance and that CGE would acquire control of **Teletra**, Fiat's US $1.4 billion-a-year telecommunications subsidiary.

OCT 4: **U.S. semiconductor and computer manufacturers** took a united stand in urging the U.S. government to seek a new bilateral five-year semiconductor trade agreement that would expand their access to the US $20 billion Japanese semiconductor market. The proposals include requiring Japan to give non-Japanese companies more than the promised 20 percent market share of chip sales as well as pressing for the dismantling of the system that now sets "fair market value" prices for Japanese memory chips.

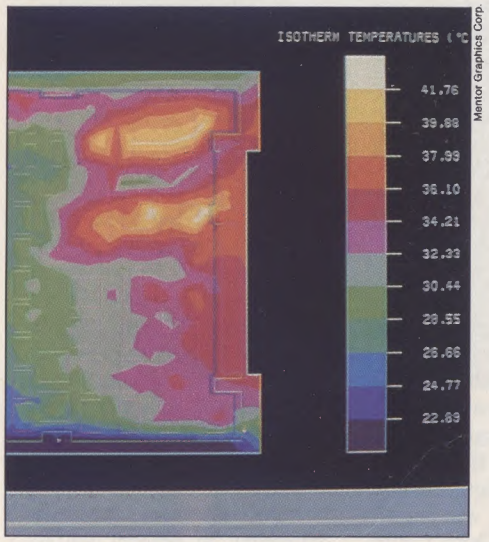
OCT 6: Breaking a trouble-plagued five-month **NASA** launching hiatus, the U.S. space shuttle **Discovery** rocketed into orbit and dispatched the **Ulysses** spacecraft on the first mission to explore the polar regions of the sun.

Preview:

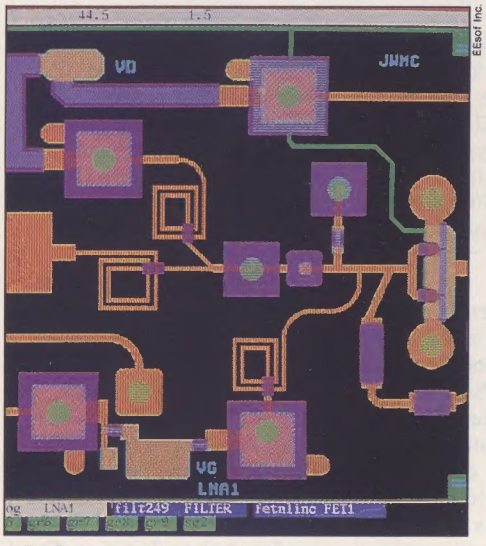
NOV. 6: Residents in Prescott, Ore., will vote today on whether to close the **Trojan Nuclear Plant** until certain conditions are met. Those include, a spokesman for Oregon's Public Utility Commission told *IEEE Spectrum*, the selection of a permanent disposal site for nuclear wastes and provision for earthquake safety. The plant is a pressurized (light) water reactor with a net capacity of 1095 megawatts.

Coordinator: Sally Cahur

IEEE
SPECTRUM
VOLUME 27 NUMBER 11 NOVEMBER 1990



73 Finite-element analysis techniques yield a board's temperature distribution



60 Analog simulations are employed to predict this circuit's performance

Spectral lines

29 **Defense issues/Legal aspects** *Donald Christiansen*
Open questions plus a new column

Focus report: engineering software

45 **Guide to offerings** *Gadi Kaplan*
52 **Digital signal processing** *Bruce C. Mather*
60 **Analog design** *John R. Hines*
68 **Electronic Design Interchange Format** *John P. Eurich, Gene Roth*
73 **Electromagnetic simulators** *Zoltan J. Cendes*
78 **Computer-aided software engineering** Spectrum *staff*
82 **Printed-circuit board design** Spectrum *staff*
86 **Displaying processed data** Spectrum *staff*
90 **User-friendly CAE** Spectrum *staff*

Special report: defense

30 **Smaller, more deployable forces** *John A. Adam*
33 **Downsizing while diversifying** *Glenn Zorpette*
37 **Defining national options** *Alfred Rosenblatt*

Applications/Tutorial

42 **Fuzzy logic design** *Kevin L. Self*
106 **Selecting microcontrollers** *John J. Vaglica*
110 **Next-generation dynamic RAMs** *Fujio Masuoka*

Management

113 **Canon: not just cameras** *Mack Chrysler*

Retrospective/Perspectives

117 **The 'blue box' phone frauds** *David Flory*
120 **The frequency that won't die** *Robert D. Barnett*
126 **Japan telecommunications quandary** *Tadao Saito*

Whatever happened to. . .?

125 **The paperless office** *William J. Spencer*

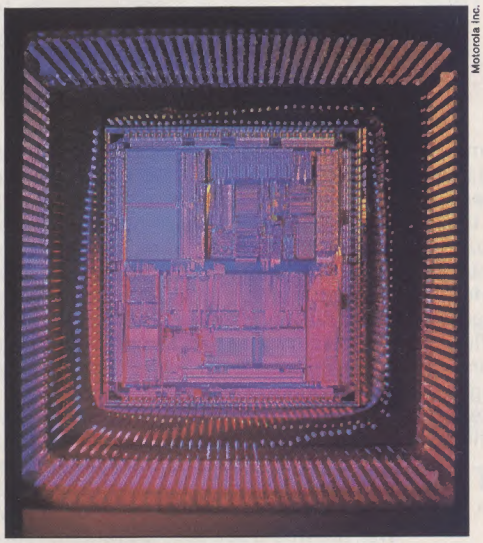
Cover: A broken sword is employed by Design Consultant Gus Sauter to symbolize the impact of the Cold War thaw on military technologies and the defense industry. A three-part report begins on p. 30.

3 Newslog
6 Reflections
8 Calendar
11 Books
14 Forum
18 Legal aspects
22 Spinoffs
24 Technically speaking
26 Managing technology
131 EEs' tools & toys
137 Reader guide
146 Scanning THE INSTITUTE
146 Coming in *Spectrum*



Canon Inc.

An assembly worker in a Canon plant in Germany inspects copier circuitry **113**



Motorola Inc.

On-chip peripherals extend a 32-bit microcontroller's versatility **106**

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What's going on?

I picture in my mind the daily travails that once filled man's workday—the hunt for shaggy, long-toothed animals, the tending of thirsty, life-supporting crops, and the sweaty manipulation of clamorous machines. But all that has passed. Today, in the midst of the information age, man fills his workday with the unending and hopeless task of trying to discover what is going on.

Just as in ancient times, my family supports me in this difficult and dangerous quest for bread to put on the table. As I go out in the morning, my dog makes a frantic rush at the front door to try to follow me. It is in part the last vestige of his hunting instinct, but he, too, has the sense of this information age imperative. He knows that things are happening out there in the great beyond—things that he will miss out on by staying at home. I can see it on his face. But no, I must face the uncertainties alone. Amidst all the dangers of the modern world, I must piece together what is going on.

When I return at night, the first thing my wife asks is, "What's going on at the office?" I usually reply, "Not much," but that belies the train of reflex thoughts that her question has provoked in my numbed brain. When my son breezes through, his first and only words are, "Hey, Pop, what's up?" Obviously, they are both deeply concerned.

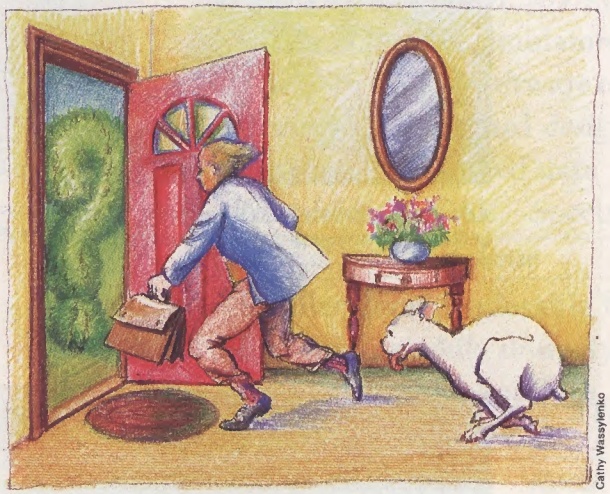
After all, what *is* going on at the office? Another day has passed in meetings, telephone calls, fax messages, electronic mail, tons of paper mail, magazines, journals, and chance meetings with associates. Something is going on—for sure. But what is it? A wisp of suspicion in my mind threatens to congeal into the ultimate disgrace of the information age: I may not be in the know.

Vacation times are especially perilous. Vacation is an unnatural state in the information age. While information continues its inexorable exponentiation—doubling every eight years or so—I remain temporarily stagnant and incommunicado. At night during these respites, I have the recurrent nightmare that I may never catch up once I get back. Some of my friends are already beginning to take fax machines on their vacations. I see the worry on their faces, too. They may miss out on something.

Even driving to work is a time of vulnerability. I used to listen to music and book tapes on my car stereo. When I mentioned having listened to a particularly interesting book to an associate, he looked at me with skepticism. "How can you listen to tapes?" he asked. "What if a nuclear war started, and you were out of touch because you were listening to recorded tapes?" Ever since he pointed this out to me, I have been uneasy about playing tapes in my car. I mean, you never know; something drastic *could* be happening.

Now I notice that my friends are installing cellular telephones in their cars. I see them pass me as they talk on these carphones. There is always a knowing look on their faces, and I am excluded. Probably something is going on.

As hard as we scramble to keep abreast of things, this is still the easiest part of our job—the data collection. The data processing is much harder. The things that we observe are the things that are *happening*.



Cathy Wassylenko

The question is: why are these things happening? For example, there is an organization change at work. The announcement goes up on the bulletin board. Then the speculation begins. What is the meaning of this change? Who and what are in? Who is out? What is the subtle message being conveyed by the notice? What is going on?

The management is frustrated by these queries. People should get back to work, they think. A second notice goes up. "The following is why this organizational change is being made . . . ," it says. However, the whole scenario is infinitely recursive, for no sooner does the second notice go up than another round of questions begins. "Why do you suppose they are telling us this?," people ask. What is *really* going on?

All this frantic activity demands a certain robust level of going-on-ness, as it were. In truth, at any given moment, there may actually be nothing going on in a particular organization.

This, however, is an unacceptable situation; in much the same way nature abhors a vacuum, these days the business world abhors an information vacuum. During this period when an insufficient number of things are going on, the speculation rises to an abnormally high level, perhaps in compensation. "What do they mean by this lull?," people ask. "Nothing has gone up on the bulletin board for the last two days," someone worries aloud. "This is surely a sign of major forthcoming revelations."

In addition to worrying about the nature of the workplace environment, the overburdened engineer has to be concerned with what is going on in technology. This is especially difficult, because most of his fellow engineers try very hard to conceal the necessary information. They publish papers in the various journals that deviously lay false trails for the readers, trying to persuade them that their papers are really part of what is going on, when in fact they have nothing to do with anything of importance.

But how are we to deduce this? The trade journals contribute to the general entropy by publishing interviews with managers and famous engineers, who give their opinions about what is going on in technology. Unfortunately, they have no idea themselves, so they make up things.

Somewhere out there, things are going on. Inventions are being made, concepts are being formulated, theorems are being proved, methodologies and processes are being conceived, markets are rising and falling, and styles are being shaped. But these things take place in a cacophony of false starts. Technology is like an orchestra tuning up. If you listen hard, you can hear little fragments of recognizable pieces. But if your attention lapses, you hear nothing but noise.

If you find out what is going on, please let me know. I am desperate.

—*Robert W. Lucky*

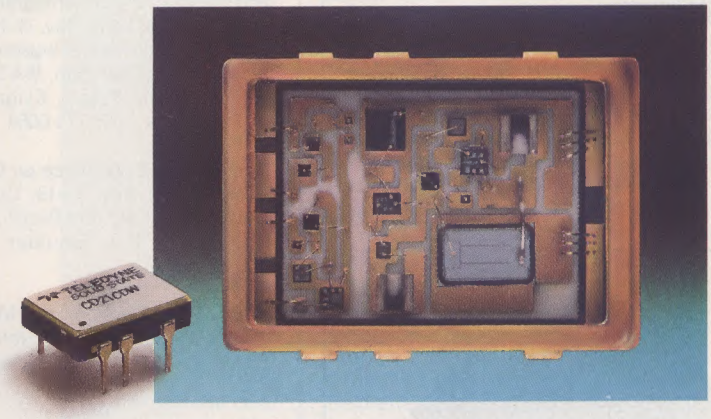
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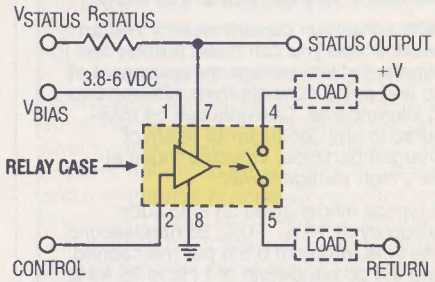
PART # CD21CDW

Review the electrical characteristics and call us for immediate application assistance.*

ELECTRICAL CHARACTERISTICS (–55°C to +105°C unless otherwise noted)				
	Min	Max	Units	
Bias Voltage (V_{BIAS})	3.8	6.0	V_{DC}	See Note 1
Bias Current (I_{BIAS})		15.0	mA	$V_{BIAS} = 5V_{DC}$
Control Voltage (V_{IN})	0	18.0	V_{DC}	
Control Current (I_{IN})		250	µA	$V_{IN} = 5V_{DC}$
Turn-Off Voltage $V_{IN(OFF)}$	3.2		V_{DC}	
Turn-On Voltage $V_{IN(ON)}$		0.3	V_{DC}	
Continuous Load Current		1.2	A	–55°C to +25°C
I_{LOAD} @ 60 VDC		0.7	A	+85°C
Output Trip Current (I_{TRIP})	2.4 (Typ.)		A	+25°C, 100ms
On-Resistance (R_{ON})		0.65	Ohms	
Turn-On Time (T_{ON})		1.5	ms	
Turn-Off Time (T_{OFF})		0.25	ms	
Status Voltage (V_{STATUS})	1	18	V_{DC}	
Status Current (I_{STATUS})		2	mA	$V_{SAT} \leq 0.3V_{DC}$ See Note 2

Notes:
1. Series resistor is required for bias voltages above $6V_{DC}$. $RS = (V_{BIAS} - 6V_{DC})/15$ mA
2. A pull up resistor is required for the status output. $R_{STATUS} = (V_{STATUS} - 0.3)/I_{STATUS}$
3. Output will drive loads connected to either terminal (sink or source).
4. Status circuit is a built-in test feature checking the input circuitry of the relay. Status output is low (on) when the input is on.

All power FET relays may drive loads connected to either positive or negative referenced power supply lines (source or sink modes).



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For additional information on hotels, conference centers, and travel services, see the Reader Service Card.

NOVEMBER

Third International Symposium on the Physical and Failure Analysis of Integrated Circuits (IEEE Singapore Section); Nov. 11-15; Westin Stamford and Westin Plaza, Singapore; IPFA 91 Technical Program Chairman, 16A Science Park Dr., No. 03-03 The Pascal, Singapore 0511; (65) 773 0056; fax, (65) 773 0054.

International Conference on Computer-Aided Design (ED); Nov. 12-15; Doubletree Hotel, Santa Clara, Calif; Pat Pacelli, 749 Clubhouse Rd., Suite 102, Boulder, Colo. 80301; 303-530-4562.

International Electronic and Materials Symposium (EDMS); Nov. 14-16; National Chiao Tung University, Taiwan; C.Y. Chang; (0+35) 720 637.

Emerging Technologies For High-Speed Digital Communications Seminar (Comm); Nov. 15; United Engineering Center, 345 East 47th St., New York, N.Y.; Jim Barbara, 212-395-8765, or Bob Putre, 914-683-3151.

Second Annual SEPRI Symposium-Industrial Electric Power Applications (PE et al.); Nov. 15-16; Doubletree Hotel, New Orleans, La.; Jack Davey, Department of Electrical Engineering, Tulane University, New Orleans, La. 70114; 504-865-5785.

Third Annual North Carolina Symposium on Artificial Intelligence (IEEE, NCSU); Nov. 15-16; Sheraton Imperial Hotel, Research Triangle Park, N.C.; Connie McElroy-Bacon or Belinda Niedwick,. Office of Continuing Education and Professional Development, North Carolina State University, Box 7401, Raleigh, N.C. 27695-7401; 919-737-2261.

International Conference on Spoken Language Processing-ICSLP (ASSP et al.); Nov. 18-22; International Conference Center Kobe, Kobe, Japan; Hiroya Fujisaki, Department of Electronic Engineering, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113, Japan; (81+3) 812 4442, ext. 6656.

Cognitiva '90 (COMP); Nov. 20-23; Madrid, Spain; IEEE Computer Society, Conference Services Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036; 202-371-1013.

Second International IFIP WG 10.2 Workshop on Electronic Design Automation Frameworks (COMP); Nov. 26-28; University of Virginia, Charlottesville; Ron Waxman, University of Virginia, Charlottesville, Va.; 804-924-6086.

Conference on Software Maintenance-CSM 90 (COMP et al.); Nov. 26-29; San Diego Hilton Beach and Tennis Resort, San Diego, Calif.; Captain Thomas Pigoski, NSGD Pensacola, Corry Station, Pensacola, Fla. 32511; 904-452-6399.

Fifth International Photovoltaic Science and Engineering Conference (ED); Nov. 26-30; Miyako Hotel, Kyoto, Japan; Hiroyuki Matsnami; (81+03) 508 1213.

Phased-Array Antennas: Theory, Design and Technology (GT); Nov. 27-29; Georgia Institute of Technology, Atlanta; Education Extension, Georgia Institute of Technology, Atlanta, Ga. 30332-0385; 404-894-2547.

23rd Annual Workshop on Microprogramming and Microarchitecture-MICRO 23 (COMP et al.); Nov. 27-29; Royal Plaza, Orlando, Fla.; C. Papachristou, Case Western Reserve University, Computer Engineering and Science Department, Cleveland, Ohio 44106; 216-368-5277.

Far-Field, Anechoic Chamber, Compact and Near-Field Antenna Measurements (GT); Nov. 27-30; Georgia Institute of Technology; Education Extension, Georgia Institute of Technology, Atlanta, Ga. 30332; 404-894-2547.

16th Annual Conference of IEEE Industrial Electronics-IECON '90 (IE); Nov. 27-30; Aslomar Conference Hall, Pacific Grove, Calif.; Robert Begun, 23609 Skyview Terrace, Los Gatos, Calif. 95030; 408-353-1560.

IEEE Central America & Panama Technical Exhibit & Convention—CONCAPAN X (IEEE Seccion Panama): Nov. 29-Dec. 1; Marriott Caesar Park Hotel, Panama City, Panama; Box 6-795, El Dorado, Panama; 507-69-3360.

DECEMBER

Global Communications Conference-Globecom '90 (COMM); Dec. 2-5; Sheraton Harbor Island Hotel, San Diego, Calif.; Andrew Cohen, Qualcomm Inc., 10555 Sorrento Valley Rd., San Diego, Calif. 92121; 619-587-1121, ext. 326.

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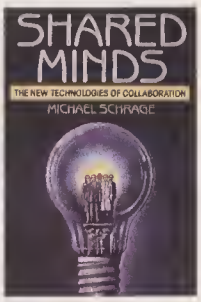
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Shared Minds: The New Technologies of Collaboration. *Schrage, Michael,* Random House, New York, 1990, 227 pp., US $19.95.



It sometimes seems as if business life has turned into one huge meeting. We spend our days huddling in conference rooms, talking with colleagues in office cubicles, playing phone tag, or catching up on office gossip around the coffee machine. About the only time interaction-saturated knowledge workers can find solitude these days is when they peer into the screens of their personal workstations.

Now, as manufacturers struggle to unite workstations and other computing devices into tools for collaboration, even this last refuge is about to disappear. The computer industry has become a battleground of buzzwords such as groupware, computer-supported cooperative work, and interpersonal computing. The result over the next decade may be a great experiment we unwittingly perform on ourselves as we attempt to blend new technologies and old collaborative habits.

This experiment is likely to lead us to question our assumptions about the nature of collaboration itself, as author Michael Schrage discovered when he set out to write *Shared Minds*. He confesses in his introduction that he intended to deliver a book about using the new technologies to collaborate more effectively, but instead he ended up exploring the nature of collaboration.

This is good news for the reader. There already are several books on collaborative technology, but Schrage has opted to hunt for more interesting and elusive game. *Shared Minds* is an engaging and insightful exploration of the nature of collaboration and how it might change in an electronic age.

Instead of constructing conceptual maps of the nature of collaboration, Schrage chooses a more practical approach emphasizing anecdotal and personal observations. By far the most provocative chapter of his book is the one titled "Collaboration," in which he interweaves these anecdotes with his insights about the collaborative process. The result is a collection of useful tips that also hint at the nature of collaboration itself.

Shared Minds is loosely organized into a baker's dozen of essay-like chapters, each focused on a different theme relevant to the intersection of technology and collaboration. The result is a book that invites browsing. I opened it with the intention of reading it from cover to cover, but, because of my interest in the relationship between linguistic theory and collaboration, quickly jumped to a chapter titled "Language matters." Then I was drawn to another chapter, "Collaboration design themes," in which Schrage offers an annotated set of elements underlying successful collaborations. I eventually read the entire book in this hopscotch fashion, with the table of contents as my reference point.

Most readers will go through *Shared Minds* in a more conventional order, but I suspect that everyone will discover a chapter or two that stands out from the rest. For example, users trying to implement groupware systems in their organizations may be drawn to chapters such as "The ecology of meetings," which details a variety of approaches to making meetings more effective. Developers, on the other hand, are likely to flip directly to "Collaboration design themes," or to "Building collaborative architectures."

The book is as valuable a reference work as it is interesting to read. Author Schrage has covered a wide territory and talked to most researchers in the field, so the curious reader will find no shortage of pointers to more detailed material. An ample bibliography and an acceptable back index enable readers to pursue leads in greater depth. I predict that *Shared Minds* itself will become a kind of groupware, with readers sharing photocopied and annotated excerpts with colleagues.

Only those impatient for a detailed map of the new collaborative terrain will be disappointed. *Shared Minds* is the first book to explore this new territory, and thus it is more suggestive than comprehensive. Schrage makes a solid attempt to outline the shape of the collaborative technologies to come, but it is simply too early for a detailed view of what remains a largely unexplored field. Schrage presents the next best thing, an honest and insightful account of his journeys through the confusing tangle of old and new. He may offer a few sketch maps, but, for the moment at least, it is up to us as readers to draw the larger map for ourselves.

—*Paul Saffo*

Paul Saffo is a research fellow at the Institute For The Future in Menlo Park, Calif., and a columnist for Infoworld Magazine.

Gallium Arsenide Digital Integrated Circuit Design. Long, Stephen, and Butner, Steven, McGraw-Hill, New York, 1990, 480 pp., US $53.95.



Even in an industry accustomed to rapid change, the advances made by gallium arsenide (GaAs) semiconductor technology in the last five years have been startling. In 1985, a commercially available GaAs circuit containing a few hundred transistors was rare. Now, GaAs integrated circuits with over 100 000 transistors are mass produced and found in mainstream computer and telecommunications systems.

This book is timely because it addresses the need to educate a new breed of circuit designer involved in this technology. In general, the volume is well organized and covers virtually all aspects of GaAs from device design to circuit design and from layout to testing and application. We especially commend the authors for the examples and problems throughout the text. The well-written solutions contain insightful explanations of the meaning and implications of the results.

The authors are undaunted by the technology's lack of standard logic families, voltage levels, or supply requirements—all complications arising from the fact that GaAs is still an emerging technology. They simply describe all the options in detail. The level of the book is just right; it assumes neither too much nor too little knowledge.

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(Continued on p. 12)

BOOKS

(Continued from p. 11)

and makes sense only as a last resort.

In fact, DCFL and its derivatives are fast becoming the dominant logic family in digital GaAs applications. Its low power dissipation makes it the only path to very large-scale integration (VLSI). The simple fact that most GaAs VLSI chips rely on DCFL circuits would seem to refute the notion that this kind of logic is peculiarly difficult to manufacture or design.

We were glad to see a chapter on interconnections with tutorial material on transmission-line theory. Many new graduates who specialized in logic design seem not to be knowledgeable in this area.

The section on test methods devotes only four pages to wafer-probing techniques, with the remainder of the short chapter covering built-in test approaches and electro-optical methods. The GaAs industry is moving toward built-in self-test very slowly. For the foreseeable future, wafer-probing will remain the dominant test strategy and for a variety of reasons, electro-optical probing will seldom be used.

With that in mind, this chapter sorely shortchanges the subject of wafer-probing. The information it does include is germane and accurate, but there is not enough detail about this difficult problem. However, the chapter cites a much better discussion, that of Strid, Gleason, and Reeder in *VLSI Microelectronics: Microstructure Science*, Vol. 11, Chapter 7, published by Academic Press in New York in 1985.

Butner and Long's discussion of built-in test approaches and structures is excellent, with design examples drawn from the literature and with some original approaches. The analysis of electro-optical probing is brief but useful.

When they review the use of GaAs in systems, the authors accurately target computers as the primary application. There is no doubt that computers will eventually become the dominant users of GaAs circuits, particularly as on-chip complexity increases. However, this section omits important applications in telecommunications, such as those in digital signal processing, automated test equipment, and digital frequency synthesis. Also, some of the problems termed "unique" to GaAs refer to antiquated processes and techniques of little relevance to modern implementations.

The section on physical design effectively illustrates and contrasts two of the major GaAs IC processes in use today. The text does assume a level of familiarity with IC processing techniques. Along with the "Magic" files included in the appendix, it is possible to get a feel for the implementation of a design in the two technologies. Since the world of GaAs ICs is rapidly changing, some updating of the rules would be necessary before an actual design is produced.

Clearly, Long and Butner have accomplished their aim—to thoroughly present GaAs digital integrated circuit design in a manner accessible to the nonspecialist in solid state. Their book should make university courses possible in GaAs IC design, and serve as a valuable reference.

—Ron Cates, Max J. Helix, and Kenneth V. Rosseau

Ron Cates is an applications engineering manager at Vitesse Semiconductor Corp. in Camarillo, Calif. He holds BS and MSEE degrees from the University of California, Los Angeles (UCLA). Max J. Helix is a process engineering manager at Vitesse. He holds a BS, MS, and Ph.D. in electrical engineering from the University of Illinois in Urbana. Kenneth V. Rosseau heads Vitesse's device and circuit modeling effort. He earned BS and MS degrees from the California Institute of Technology in Pasadena and a Ph.D. from UCLA.

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RECENT BOOKS

Numerical Analysis. *Elden, Lars, et al.*, Academic Press, New York, 1990, 347 pp., $39.95.

Software Engineering for Electronic Systems Designers. Ed. *Jenkins, D. G., et al.*, Peter Peregrinus, London, 1990, 304 pp., $65.

Waves and Fields in Inhomogeneous Media. *Chew, Weng Cho,* Van Nostrand Reinhold, New York, 1990, 611 pp., $56.95.

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Analogue IC Design: The Current-Mode Approach. Ed. *Toumazou, C., et al.*, Peter Peregrinus, London, 1990, 646 pp., $85.

Principles of Optical Engineering. *Yu, Francis T. S., and Khoo, I. C.*, John Wiley & Sons, New York, 1990, 311 pp., $49.95.

Theory and Design of Concrete Shells, 3rd Edition. *Chatterjee, Binoy K.*, Chapman & Hall, New York, 1990, 280 pp., $80.

Microsoft Excel. Ed. *Kyd, Charles W.*, Microsoft Press, Redmond, Wash., 1990, 578 pp., $24.95.

The Best Book of Microsoft Windows 3. *Townsend, Carl*, Howard W. Sams, New York, 1990, 440 pp., $24.95.

Artificial Neural Systems (Foundations, Paradigms, Applications, and Implementations). Ed. *Simpson, Patrick K.*, Pergamon Press, New York, 1990, 209 pp., $39.50 (hard); $19.50 (soft).

Interfacing to the IBM Personal Computer. *Eggebrecht, Lewis C.*, Howard W. Sams, New York, 1990, 345 pp., $21.95.

Data-Directed Systems Design: A Professional's Guide. *Modell, Martin E.*, McGraw-Hill, New York, 1990, 324 pp., $39.95.

The First Book of PC-Write. *Kenyon, Rebecca*, Howard W. Sams, New York, 1990, 352 pp., $16.95.

Rogue Programs: Viruses, Worms, and Trojan Horses. Ed. *Hoffman, Lance J.*, Van Nostrand Reinhold, Florence, Ky., 1990, 384 pp., $32.95.

RISC Systems. *Tabak, David*, Research Studies Press, John Wiley & Sons, New York, 1990, 300 pp., $44.95.

The First Book of Draw Perfect. *Baake, Susan, and Kelly, James Kevin*, Howard W. Sams, New York, 1990, 330 pp., $16.95.

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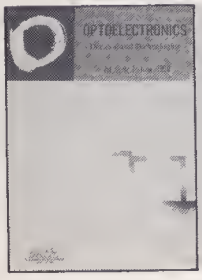
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Circle No. 4

Tactics or chores?

It seems to me that the pilot's associate discussed in "Computer-aided fighter pilots" [March, p. 38] would be most useful if it concerned itself with things the pilot paid no heed to. For example, according to James Fallows' book *National Defense* (Random House, New York, 1981), three F-4s were lost because the pilots were so intent on chasing MiGs, they ran out of fuel. A pilot's associate might have prevented that by monitoring the fuel state, but not by assisting them in catching their quarry.

There are no "optimal" tactics, because surprise is of paramount importance, if only because it can disconcert the opponent. A computer program's tactical maneuvers will be stereotyped and predictable if the opponent has obtained the algorithm, either through espionage or reverse engineering from the reports of encounters. I therefore find it implausible that a program would be very useful in advising about tactics.

Louis Baker
Albuquerque, N.M.

More on Thévenin's theorem

James E. Brittain's article on Thévenin's theorem [March, p. 42] is well done, but the lower Box A might have appeared in two versions as



and been more readily understood.

A bit more history may be of interest. It seems correct to credit Bell Laboratories' sources with popularizing the theorem; K. S. Johnson's *Transmission Circuits for Telephonic Communication*, 1925, devotes most of a short chapter to the theorem. This book was intended for internal Bell teaching, and the theorem was not generally in print until Everitt's *Communication Engineering* appeared in 1932. Even Guillemin V II, *Communication Networks*, 1935, presents it only as part of a problem on p. 181.

I may have been responsible for its use to describe an induction motor. While teaching communication circuits in 1944 at Iowa State, one of the machinery professors, B. S. Willis, sat in my class and saw the advantages of Thévenin's theorem, and later reworked some of his induction motor material. He subsequently published on the subject.

As late as 1949, I was told by a power professor that Thévenin's theorem had no place in circuits work.

Everitt, in a personal communication, told me that he was the first to publish Norton's theorem, which he had found circulating as a memo during his summer employment at Bell Laboratories in 1926.

Since it took so many years for Thévenin's work to reach its proper eminence, it is not surprising that Helmholtz has not yet received his due. The fact that the original papers were in French says little for the abilities of electrical engineers to read a foreign language, circa 1930. Even the Massachusetts Institute of Technology, in including German in its first curriculum in 1882, perhaps made a bad guess (see J. D. Ryder and D. G. Fink, *Engineers and Electrons*, 1984, p. 194).

John D. Ryder
Ocala, Fla.

Brittain deserves much credit for strongly bringing out that Thévenin's theorem was published much earlier by Hermann von Helmholtz. With reference to Norton's theorem, Brittain correctly refers to Mayer. If, however, we were to agree that the true originator of a theorem is the one who publishes it first, then we would end with a von Helmholtz-Mayer theorem instead of a Thévenin-Norton theorem. While Mayer published his theorem in 1926, that same year Norton's theorem appeared only as part of a Bell Telephone Laboratories patent communication; it was not published until many years later.

As one of the reviewers of the Brittain article, I had the opportunity to propose that whenever there is a disagreement about the identity of the originator of a theorem, the theorem should be named with reference to its content, with no originator's name stated. Then we end up with only two theorems: the "Equivalent Generator Theorem" and the "Source Transformation Theorem." Since the latter is contained in the former, future EE students need only learn one theorem, which, so to speak, does everything and even includes dependent sources, unless coupling exists.

The quotation from Dorf's book states that in Norton's theorem, the current source is paralleled by a resistance. Actually, Norton stated that it is connected in parallel with an *impedance*. With that formulation, Norton opened the door to the treatment of storage elements, in both the steady state and the transient state. Norton thus, in 1926, took a monumental step forward in network theory, and those using Thévenin's and other theorems formulated only for the resistive case soon followed his lead.

Harry E. Stockman
East Dennis, Mass.

The author responds: In the original version of the article, I included some discussion of the 1925 book by Kenneth S. Johnson and of the role of Aime Vaschy and George A. Campbell in the dissemination of the theorem. (Campbell had studied in France after graduating from MIT and could read the Vaschy treatise of 1890 that included the theorem.) Space limitations precluded the publication of the information.

Europe 1992

I feel that the statement of Georges Van der Perre, the SEFI (European Society for Engineering Education) representative [June, p. 47], concerning how various engineers will be affected by a directive setting professional standards, was incomplete.

The point of view of Claiu (Liaison Committee of the Associations of University Graduate Engineers of the European Community) is that in Europe, except perhaps in the United Kingdom and Ireland, two tracks in engineering education (for example, French Grandes Ecoles versus West German Fachhochschulen) also imply two strongly different levels and orientations in lifelong professional qualification for the individual. In that context, there is no room for a converging "end product" that some factions within Féani (European Federation of National Engineering Associations) seem to advocate.

I want also to emphasize that not only engineers working as civil servants or self-employed engineers ("independent" consultants) but also privately employed engineers will be directly affected by the general directive and by an eventual complementary special directive as well.

In fact, the preamble to the general directive stipulates: "... this means in particular the possibility of pursuing a profession, whether in a self-employed or employed capacity, in a Member State other than that in which they acquired their professional qualifications."

R. de Bruyn
Antwerp, Belgium

Corrections

On p. 26 of the July issue and p. 18 of the August issue, the frequencies for today's cordless telephones should have been 49 MHz and 46 MHz.

On p. 50 of the August issue, the first word, Japan, should have been deleted. In the table on p. 51, the second "GHz" should have been deleted from the phrase "1.5 GHz for maritime GHz" in the box labeled "Technology introduced" for Intelsats V and VA. On p. 51, the last word of the fifth line should have been TDMA. In the first full paragraph on p. 52, the correct name for Inmarsat should have been International Maritime Satellite Organization; the correct name for AMSC should have been American Mobile Satellite Corp.

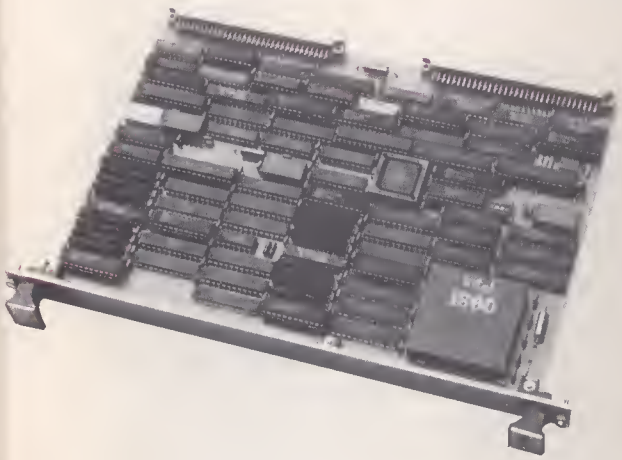
—Ed.

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Software copyright protection extended

At one time, it was assumed that the copyright for a computer program covered only the software code. This line of thinking allowed a software designer to safely emulate the look and feel of a competitor's program if he independently wrote his own code. But that notion has been eroding quite rapidly in the face of increasing protection for "non-literal" elements of software—that is, components not literally embodied in a program's coding.

A recent Federal district court decision, *Lotus Development Corporation v. Paperback Software International*, dramatically illustrated the direction in which some courts are moving. At issue were the structure, sequence, and organization of the menu command system in the well-known Lotus 1-2-3 computer spreadsheet. In a 113-page opinion, U.S. District Court Judge Robert E. Keeton ruled in late June that these form a copyrightable, non-literal element of the Lotus 1-2-3 program, and that a competing spreadsheet program, VP-Planner, infringed the Lotus copyright.

The lawsuit was first filed in January 1987, when Lotus Development Corp., Cambridge, Mass., sued two companies, Paperback Software International Inc., Berkeley, Calif., and Stephenson Software, Ltd., Vancouver, B.C., for copyright infringement. Stephenson had developed VP-Planner, which Paperback helped publish and market. Lotus argued that the Paperback product incorporated the same distinctive user interface that Lotus offered, consisting of specific menus, long prompts, function key assignments, and macro commands.

Paperback countered that a user interface could not be protected by copyright, because the interface represented non-literal elements of the program. That is, features such as the menu command system's organization were not literally embodied in the code of the Lotus 1-2-3 program. Lotus, however, took the position that such elements were indeed part of the copyrighted work and thus protected.

Idea v. expression

After reviewing the history of copyright law and certain recent cases, the judge devised a test for determining whether the user Lotus 1-2-3 interface was protectable by copyright. He warned, though, that this test was merely an aid in focusing on relevant factors.

His analysis began with the fundamental principle of copyright law: that one may not copyright an idea but only the rendering or "expression" of that idea. In the context of the *Lotus v. Paperback* case, the "idea" of a spreadsheet does not qualify for protection, but a particular version of a spreadsheet may do so.

The test fashioned by Judge Keeton has three parts. First, it defines the idea behind the work—in this case, a computer program—as an abstract concept separate from its expression. Such a distinction is subjective, but necessary to help determine the parameters of a copyright.

Second, the test determines whether a computer program is limited to particular elements essential to the expression of the basic concept, or whether it is simply one of many possible ways of expressing that concept. Here the goal is to discover whether the Lotus 1-2-3 program included "identifiable elements" not essential to every expression of the concept of a spreadsheet. If the "expression" is limited to particular essential elements or few variations, then the courts hold that the expression "merges" with the idea, and copyright law prohibits any one company or individual from acquiring exclusive rights to that expression.

For example, suppose an exit sign in a screen display is used to represent the function of leaving a program. A court would probably not permit a copyright on that symbol, on the grounds that it directly represents the idea of an exit and thus "merges" with the idea itself. If, on the other hand, the expression is only one of many ways of presenting the concept—for example, a picture of a doorway—a court would look more favorably upon copyright protection for such a symbol.

Third, the judge's test asks whether the identified non-essential elements form a "substantial part" of the work, thus entitling them to copyright protection. This third part also requires a subjective determination by the judge.

Judgment 1-2-3

Applying this three-part test, Judge Keeton examined the various elements of VP-Planner that Lotus contended were wrongfully appropriated. In part one—the program as an abstract concept—the judge discussed the concept of an electronic spreadsheet. He concluded that while spreadsheets *per* se are not copyrightable, not every form of a spreadsheet is obvious and, therefore, some aspects may be protectable by copyright.

With Lotus 1-2-3, the judge held that specific features of the user interface might contain copyrightable subject matter. Likely prospects included the rotated-"L" display, the designated key invoking the command system, the arithmetic function keys, and the structure, sequence, and organization of the menu command system. He concluded that these features themselves represent abstract concepts, separate and apart from the actual expression of the spreadsheet program, and he therefore examined them in the context of the remaining two parts of the test.

In the second part of the test— identifying the non-essential program elements that implement those abstract concepts—the judge found that the rotated-"L" display is widely used in spreadsheet programs. Further, a designer might choose to invoke any particular command by one of only a few obvious keys, so that the concept of the command necessarily merges with the idea of such a key. Finally, the arithmetic function keys used by Lotus 1-2-3 are obvious. Thus, the judge deemed the rotated-"L" display, the designated key invoking the command system, and the arithmetic function keys not copyrightable.

The structure, sequence, and organization of the menu command system, however, are "capable of being expressed in many if not an unlimited number of ways...," Judge Keeton stated in his opinion. He found that the choice, structure, and order of the command terms; the presentation of the commands on the screen; and the long prompts were unique to Lotus and therefore copyrightable.

Moreover, the judge viewed the command structure as an integral whole, commenting that even if the individual elements may be obvious, their obviousness would not preclude copyright protection for the "whole" expression.

Finally, in part three of his test, "whether the structure, sequence, and organization of the menu command system is a substantial portion" of Lotus 1-2-3, the judge unequivocally concluded that it was.

He also noted that major portions of this aspect of Lotus 1-2-3 had been intentionally copied by Stephenson, as revealed in part by an affidavit of James Stephenson, the founder of Stephenson Software. In addition, the instruction manual declared, "VP-Planner is designed to work like Lotus 1-2-3, keystroke for keystroke....VP-Planner's worksheet is a feature-for-feature workalike for 1-2-3. It does macros. It has the same command tree. It allows the same kind of calculations, the same kind of numerical information. Everything 1-2-3 does, VP Planner does." The judge's conclusion that there had been deliberate copying of features of the Lotus product undoubtedly influenced his decision.

The legacy of Lotus

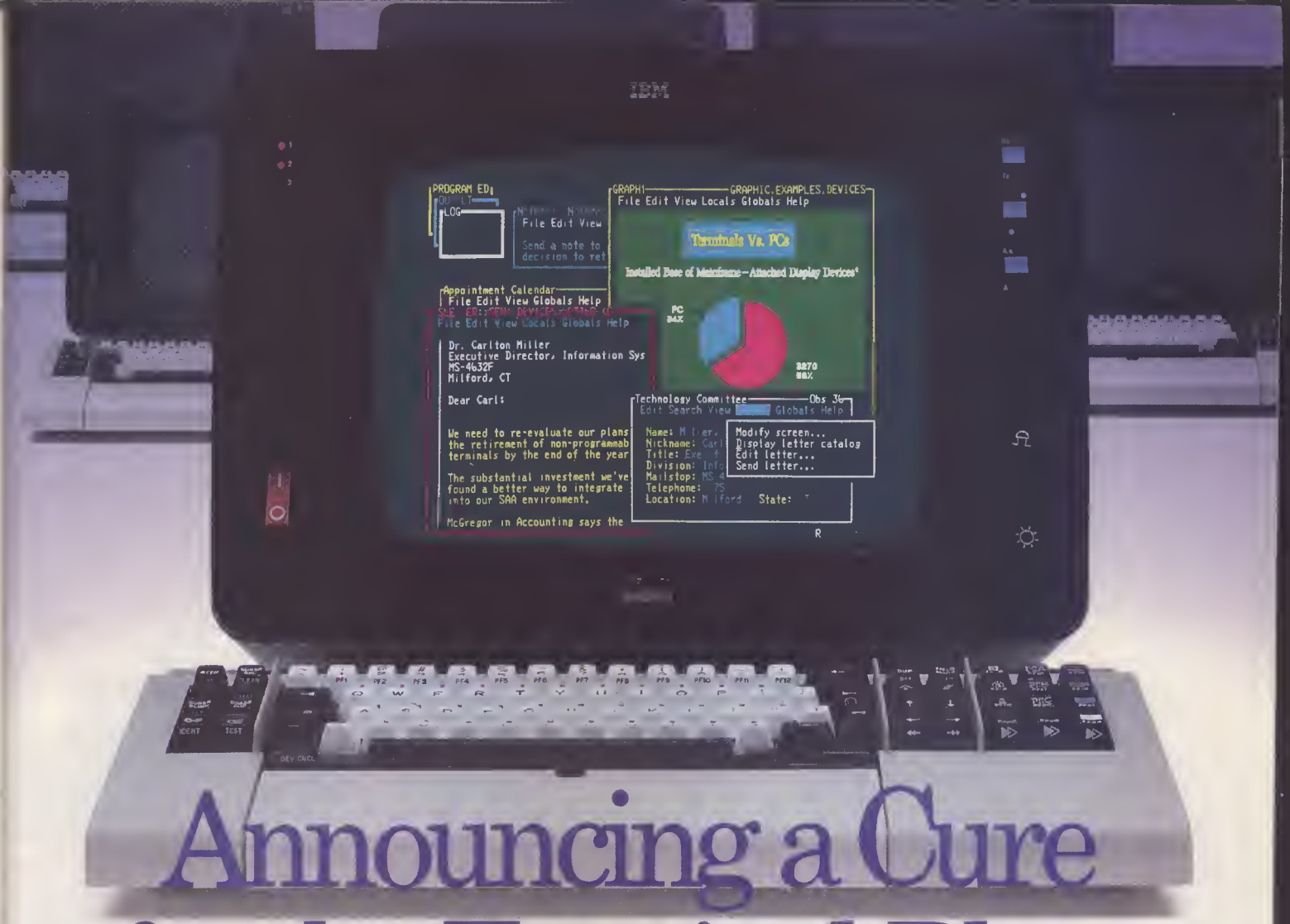
Of several procedural defenses raised by Paperback and Stephenson, one deserves mention here. The companies contended that Lotus' registration covered only the coding for the program and not the "screen displays." Judge Keeton ruled, however, that the registration of the "entire work" sufficed to protect the displays.

As Judge Keeton's opinion is at the trial court level, the companies could appeal his decision. According to an article appearing in *Computerworld* on July 2, 1990, Paperback Software has indicated that indeed it would appeal this far-reaching decision. If allowed to stand, the court's opinion will influence software design, as it will affect virtually every user-oriented applications package.

Judge Keeton emphatically stated, however, that his test was not to be taken as a fixed set of rules to be used to determine copyrightability in future cases, although other courts may likely adopt the judge's test. Nonetheless, each situation will depend on the facts and, therefore, the next case will have to be judged on its own merits.

—*Joel Miller*

Joel Miller is an attorney at the New York City law firm Weil, Gotshal & Manges.



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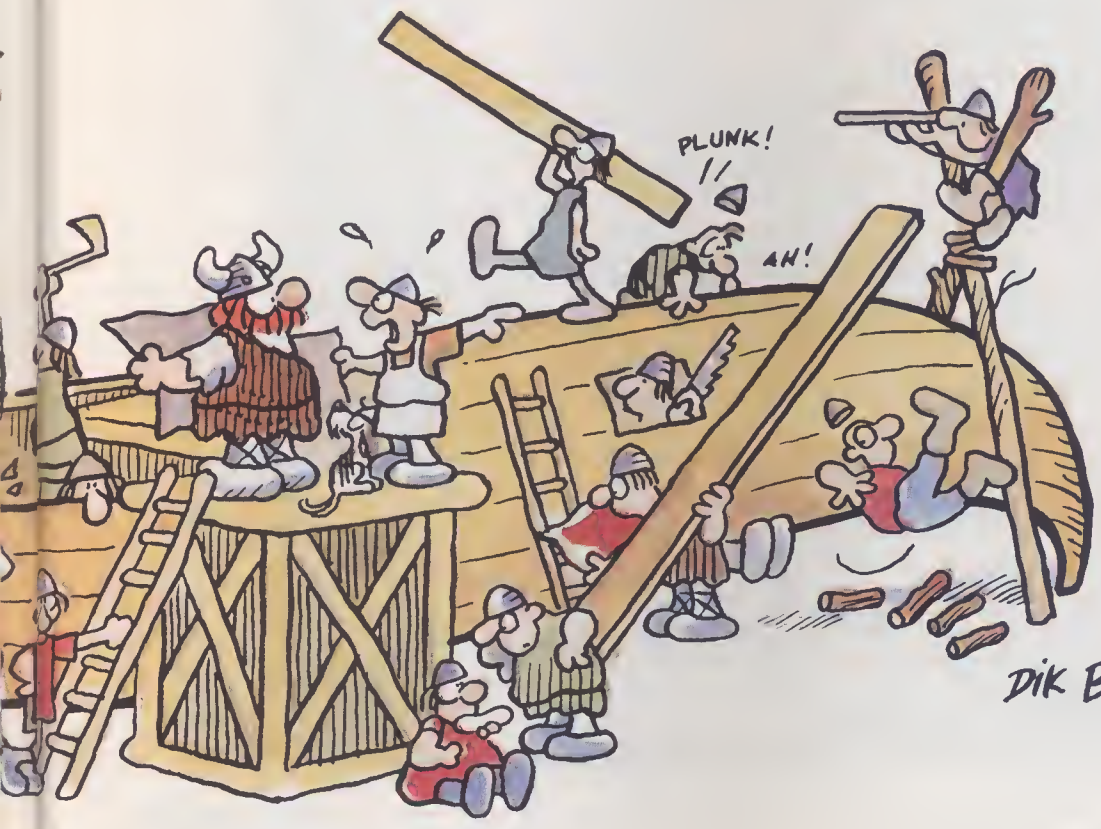


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Third International Conference on Computer Vision-ICCV '90 (COMP); Dec. 4-7; Miyako, Asahi Plaza, and I-House hotels, Osaka, Japan; ICCV '90, IEEE Computer Society, Conference Services, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036; 202-371-0101.

29th Conference on Decision and Control (CS); Dec. 5-7; Hilton Hawaiian Village, Honolulu, Hawaii; Malcolm D. Schuster, RF-23-377, Johns Hopkins University, Applied Physics Laboratory, Laurel, Md. 20707.

Ultrasonics Symposium (UFFC); Dec. 5-7; Sheraton Waikiki Hotel, Honolulu, Hawaii; Moises Levy, Physics Department, University of Wisconsin, Milwaukee, Wis. 53201; 414-963-4168.

Fourth International Workshop on CASE-CASE '90 (COMP et al.); Dec. 5-8; Irvine Hilton and Towers, Irvine, Calif.; Ronald Norman, San Diego State University, College of Administration, San Diego, Calif. 92182; 619-594-3734.

21st Annual Semiconductor Interface Specialists Conference (ED); Dec. 5-8; San Diego Hilton Beach and Tennis Resort, San Diego, Calif; Steve Lyon, 609-258-4635.

International Electron Devices Meeting (IEDM/IEEE); Dec. 9-12; San Francisco Hilton and Towers; Melissa Widerkehr, IEDM 1990, 655 15th St., N.W., Suite 300, Washington, D.C. 20005; 202-347-5900.

Second IEEE Symposium on Parallel and Distributed Processing-SPDP (COMP); Dec. 9-13; The Colony Parks Hotel, Dallas; Behrooz Shirazi, Department of Computer Science and Engineering, Southern Methodist University, Dallas, Texas 75275-0122; 214-692-2874.

San Diego Workshop on Volume Visualization (COMP et al.); Dec. 10-12; San Diego Supercomputer Center, La Jolla, Calif.; T. Todd Elvins, SDSC, Box 85608, San Diego, Calif. 92018; 619-534-5128.

Workshop on Heterogeneous Database Systems (COMP); Dec. 11-13; Northwestern University, Evanston, Ill.; IEEE Computer Society, Conference Services, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036; 202-371-1013.

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Fourth CSI/IEEE International Symposium on VLSI Design (COMP et al.); Jan. 5-8; New Delhi, India; Y.K. Malaiya, Computer Science Department, Colorado State University, Fort Collins, Colo. 80523; 303-491-7031; or D. Roy Chowdhury, Gateway Design Automation, SDF- A-1, Noida Export Processing Zone, P.O. NEPZ, Noida-201305, UP, India; (91+57) 366 2342.

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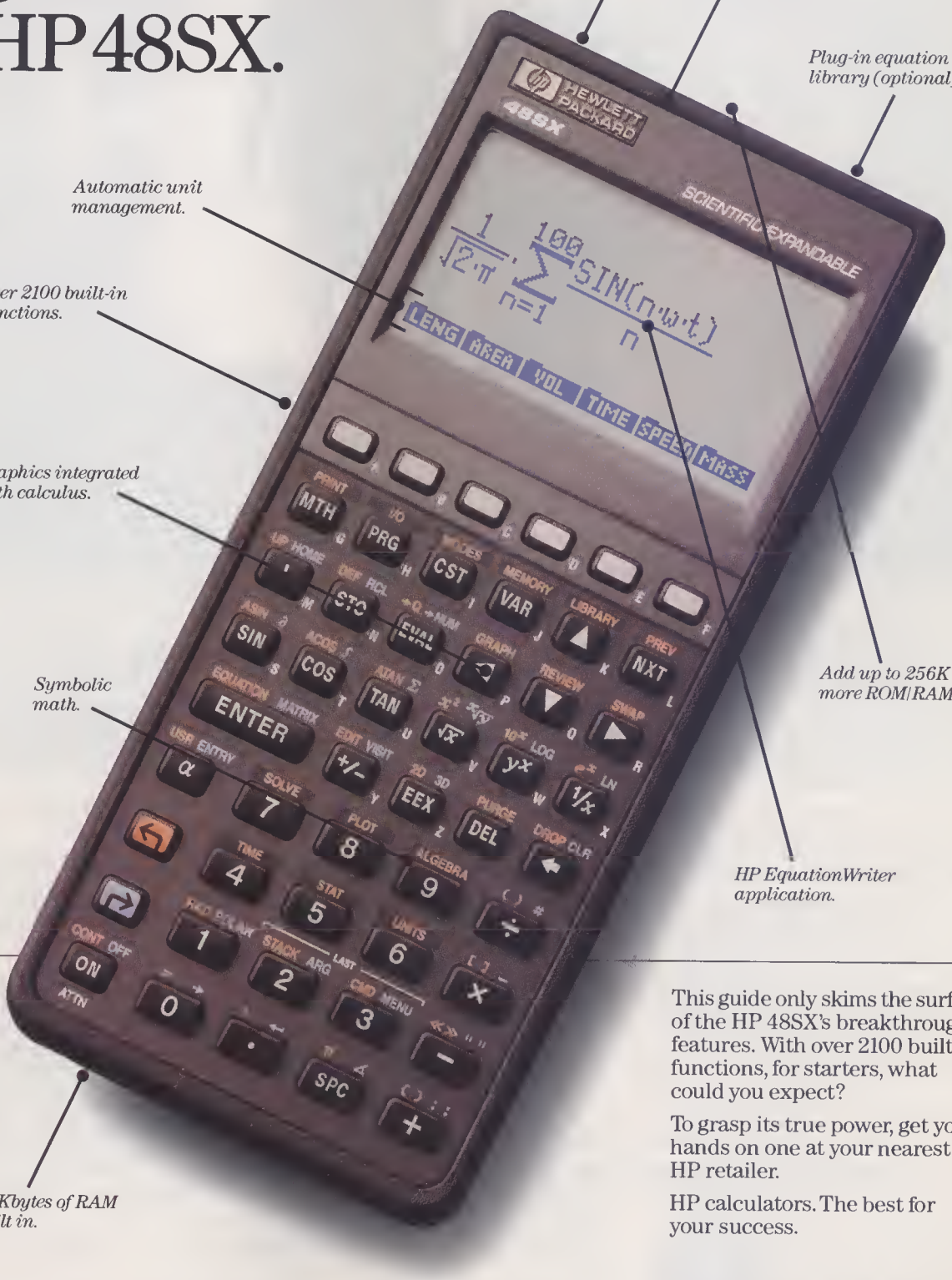
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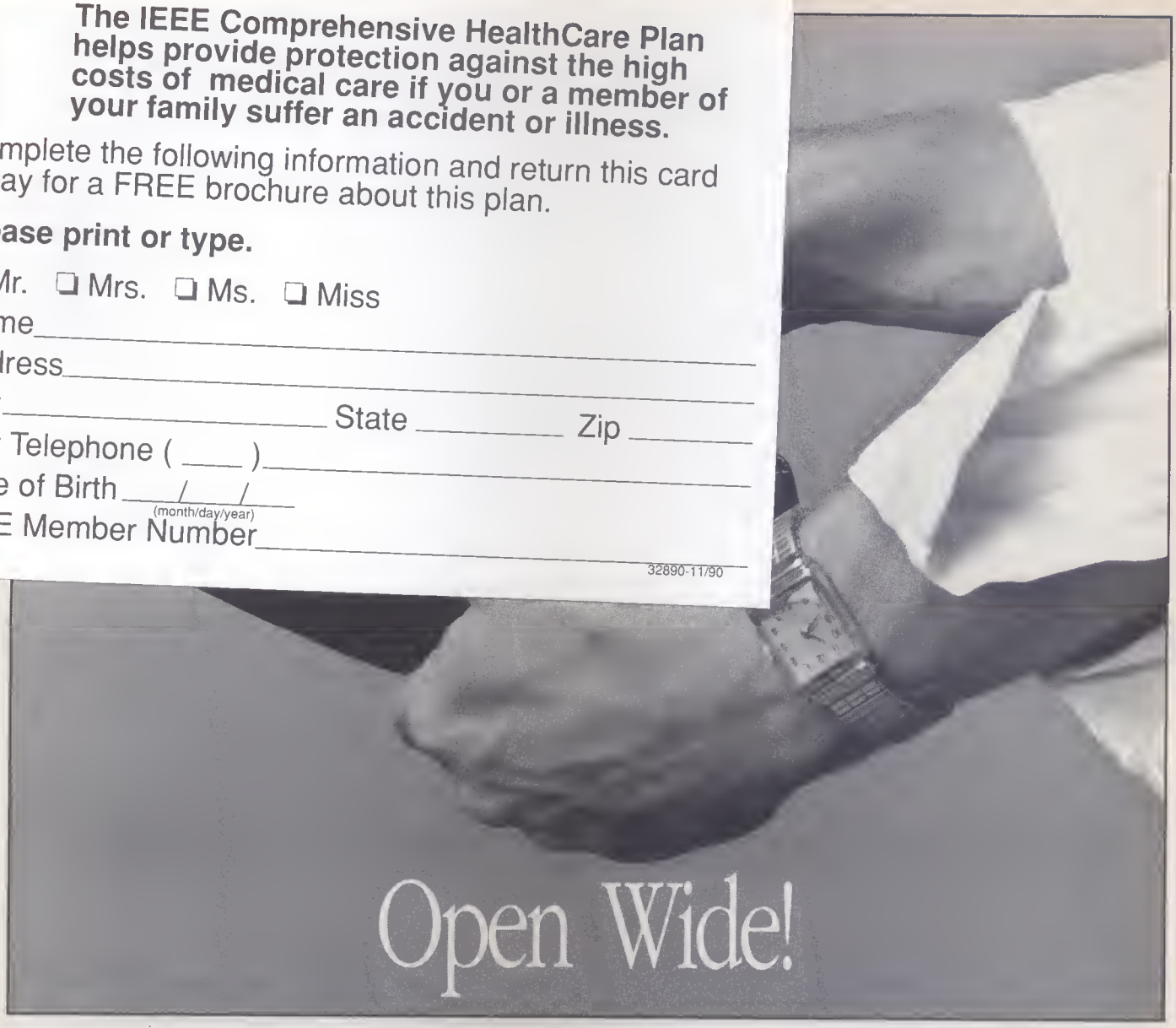
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A hi-tech approach for grading meat

Australian beef exporters and American hog researchers are benefiting from a labor-saving device first commercially available in 1985 for accurately measuring bodyfat in people. Both the Brisbane and the Purdue University, West Lafayette, Ind., groups are using a variant of the original electromagnetic scanner to measure the



amount of lean tissue and the lean-to-fat ratio of each carcass or product container.

Manufactured by Meat Quality Inc., Springfield, Ill., the US $85 000 system, Model MQ-25, can scan one carcass or box of meat every four seconds as it passes through a tunnel on a conveyor belt, according to Robert Funk, vice president of engineering.

The carcass passes through an electromagnetic field, where a detector measures changes in the electrical properties. Because fatty tissue contains virtually no electrolytes compared to lean tissue, the detector can determine the amount of lean tissue and adjust it for the mass of the carcass. The method in use before—visual inspection—was slower and less accurate.

The original device, the Total Body Electrical Conductivity (TOBEC) from EM-Scan Inc., also in Springfield, has been used for nutritional studies by Marta Van Loan, a research physiologist at Western Human Nutrition Research Center, San Francisco, and some 20 other research groups.

Zapping hearts

About 3 out of every 1000 persons suffer from tachycardia, when their heart may beat three to four times faster than normal (60–80 beats per minute). In some cases the attacks are fatal.

For about a year, a radio wave technique has been employed to treat two types of tachycardia by three medical professors: Jonathan Langberg, now at the University of Michigan, Ann Arbor, but until recently at the University of California in San Francisco; Warren Jackman at the University of Oklahoma, Oklahoma City; and Fred Morady, also at Michigan, and their colleagues. Previously, doctors applied several kilovolts for several milliseconds to the heart through a defibrillator.

The approach, called RF catheter ablation, obviates surgery, pacemakers, medication or the more painful defibrillator. It cauterizes areas of the heart to shut off the extra channels of electrical connection that cause the condition. In the procedure, a cardiologist inserts wires through a vein in the leg to various locations of the heart. After mapping the heart and taking internal electrocardiogram readings from each site, he or she can narrow down the problem area.

Once the vicinity of the extra conductor is determined, the doctor places the wire at the site while watching an X-ray monitor. RF waves of 100 to 500 kilohertz pass through the wires for 10 to 60 seconds to heat the tissue at the catheter end and destroy the conductor, said Langberg, an associate professor of medicine at the university.

In the case of atrioventricular nodal re-entry tachycardia, a normal path is split into two paths. With the more severe Wolff-Parkinson-White syndrome, the extra conductor is apart from other conductors. As both conditions are congenital, many patients are young.

The entire procedure takes two to four hours and requires 48 hours' convalescence. Surgery would require a week in the hospital and several weeks for recovery. The procedure is considered investigational, so that patients are not yet charged full fees; but Langberg believes that it would cost about half as much as heart surgery.

Using radio waves as a source is also more desirable than using a defibrillator for several reasons: it is safer, less painful, and easier to control, Langberg said. "The old method was associated with infrequent but potentially serious side effects such as gas formation, explosion, perforation, and low blood pressure," he said.

Langberg, Morady, and their colleagues at the University of Michigan have cured about 85 percent of 170 patients in the past year. They hope to make the procedure available on an out-patient basis.

One limitation of the approach is that it can cauterize areas up to 3–4 square millimeters only. For conditions such as ventricular tachycardia, in which an area the size of a dime is affected, the radio frequency treatment is not useful, said Langberg, who is investigating using a microwave antenna as a power source.

Monitoring fetuses

A Welsh company, Huntleigh Technology PLC, Cardiff, has developed a handheld fetal monitor for expectant women. Clinics in developing countries may also be interested in the pocket-sized monitor because of its relatively low price, US $625. Full-sized versions, about the size of attache cases, detect fetal heartbeats as well as contractions and changes of electrical potential. They cost between US $4000 and US $11 000.

Called Fetal Dopplex, the battery-powered device applies the same ultrasonic technique as much larger versions found in hospitals. The monitor detects heartbeats in fetuses at least 10 weeks old. It displays the readings on a liquid crystal display and amplifies fetal pulse sound through a built-in loudspeaker. The fetal rate of a healthy fetus beats 120–160 times a minute.

A spinoff of the fetal monitor is the company's Bidirectional Pocket Doppler, the first handheld flowmeter that allows doctors to diagnose varicose veins, venous ulcers, and atherosclerosis. The device, which sells for US $750, indicates the velocity of flow audibly, by pitch, and visually, by up to three arrows. The arrows also signal the direction of flow.

Controlled drying

Radio frequency waves are also being used to dry plasterboard to perfection. Used in large sheets as a backing or a substitute for plaster in walls, the material is at present subjected to a 120-meter hot-air dryer that heats it to 400–600 °F (120–320 °C), often overdrying it and removing water from the gypsum in the material.

The RF method was devised by Philip Schmidt, director of the Process Energetics Program at the University of Texas at Austin, and his colleagues. RF drying is being used commercially in preparing other products, such as food, plywood, and paper, but it is still in laboratory development for plasterboard, he said. For all these applications, RF heating is used in the final drying stage after hot-air drying.

Schmidt, who is also director of the Texas Drying Research Consortium, used 27 megahertz waves to dry the plasterboard. The waves do not affect the bound molecules in the gypsum, only the free water molecules, causing them to rotate quickly to generate energy for drying the material, so that overdrying was not a problem.

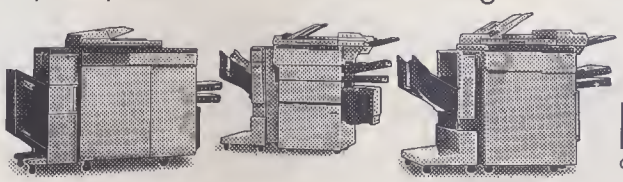
What will determine whether RF drying will be used commercially to prepare plasterboard is simple economics, Schmidt said. Compared to the products that are being dried by RF waves, plasterboard is cheap. A 4-by-8-inch (10-by-20-centimeter) piece of plasterboard costs only US $2.50–$8.00. Using electricity to dry the product for 5 minutes after 30 minutes of hot-air heating by gas may not be economical compared to 45 minutes of just hot-air heating. On average, about 4–5 percent of the plasterboard is lost using hot-air heating, Schmidt said.

Schmidt and his colleagues are looking into other applications of RF heating that have more added value, such as pet food processing.

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Just when you thought it was safe. . .

The market for new, often nonsensical words has slowed down recently, having reached its zenith in 1988, with gems like *productization* and *nomenclatured*. But things are looking up again. A recent speech by Dugald K. Campbell, vice president and general manager of Siemens Automotive's Sensor Systems Division, yielded three new "words" that he termed "paradoxes" of the globalization of the supplier industry.

One of these is *glocalization*, which refers not only to a company's need to produce in volume for the global market, but also to customize its products for local customers at nearby plants. Another, *coopetition*, describes relationships between companies that compete but still cooperate to develop a technology useful to each; it also extends to joint efforts between a company and a customer to develop a technology the customer needs, although the company is forbidden from offering it to other customers. The third, *technostriction*, occurs when a company must choose from among many worthy technologies the one in which it will invest R&D funds and efforts.

These are certainly paradoxes, but is it really necessary for them to be described in a single word, especially when that word needs considerable explanation?

Pronouncing the unpronounceable

With the ever-increasing use of abbreviations in the electronics industry and other areas, the tendency to pronounce the bizarre "words" formed by the abbreviations has grown. Pronouncing them as words rather than saying each letter is usually shorter and less cumbersome and may make them a bit less intimidating.

But some of the words turn out to have rather unsavory connotations. For example, the small-computer system interface (SCSI) is pronounced *scuzzy*, which is also a slang term meaning unkempt or disgusting. SDI, the abbreviation for the Strategic Defense Initiative, could be pronounced *sidi* or *seedy*, another word with unfavorable connotations. The American National Standards Institute (ANSI) is called *ansy*, which sounds like *antsy*.

But most of these words simply sound nonsensical or, at best, quirky. What-you-see-is-what-you-get (Wysiwyg) translates into *wizzywig*, which could perhaps be interpreted as an expression indicating approval of one's head-covering. The philosophy of not-in-my-backyard is *nimby*. Very high-speed IC (VHSIC) becomes *vissic*. The Electronic Design Interchange Format (EDIF) is *eedif*, while the Initial Graphics Exchange Specification (IGES) becomes *ijes* (with a long i). But computer-aided engineering (CAE) could be pronounced *say* or *kay*.

Some other abbreviations are pronounced as a combination of single letters and words. For example, dynamic random-access memory (DRAM) is usually pronounced *deeram* rather than *dram*, a word meaning a small helping of a beverage. The Joint Test Action Group (JTAG) is spoken of as *jaytag* rather than *jettag*, a nonsense word like *nimby*. And the Product Data Exchange Standard (PDES) is pronounced *peedes*.

There are some abbreviations, however, that would be all but impossible to pronounce. Take, for instance, the Very High-Speed Hardware Description Language (VHDL). What would it sound like? *Vodel*, perhaps? Let's face it: some abbreviations cannot be improved by pronouncing them.

A long time b.p. . .

The New York Times is generally considered the newspaper of record—in the United States, at least. If the *Times* does indeed have a pervasive influence, then the abbreviation *b.p.* may soon become a part of the working vocabulary.

Recently, *b.p.* appeared in a diagram accompanying an article in the *Times*' science section on the migration of giant ice sheets over the last 120 000 years. Its meaning? *Before the present*. The expression is not used in the article itself, where just one word was used to convey the same meaning: *ago*.

That's the thanks you get

A reader Edward W. Harding noted that in the *Spectrum* article, "A continent bound by wire" [August, pp. 58–59], the task of cutting poles for the U.S. transcontinental telegraph system under construction in the early 1860s was described as *thankless* because of the lack of trees on the Midwestern prairies.

Harding was understandably puzzled. 'If the prairie was treeless, it might be an extremely difficult task, it might be an impossible task, but how could it be a task for which one would get no thanks?' he wrote. Indeed, *thankless* does not convey the point the author was trying to make. *Difficult* might be a better word, as Harding suggested, or perhaps *arduous* or *strenuous*.

Actually, Technically Speaking has no idea whether anyone thanked the pole-cutters but certainly hopes so.

Driving writers crazy

Those who write about automotive technology are often seized with an irresistible urge to commandeer automotive cliches as metaphors for actions that would be described differently if the subject was something other than automobiles. A couple seen recently are:

- "Electronics: moving into high gear"
- "Cars will take semis for a ride in the '90s"

This publication has not been immune, either. A few headlines from *IEEE Spectrum* include:

- "Looking down the road" (automotive projections)
- "The automobile: it's the super-driver of both technology and society"
- "Technology on wheels"

Here is a handy list to scan next time you have to deal with an automotive topic:

- takes a back seat
- veering in new directions
- putting the brakes on
- shifting gears
- careening
- gets the green light
- spins its wheels
- runs out of gas

Perhaps when you see these lined up together like one big traffic jam, you may decide to take another route. It's about time this overuse of automotive metaphors came to a screeching halt.

A 'quantized' baby

A Japanese solid-state researcher, who shall remain unnamed here, was chatting amiably with U.S. reporters at an international technical conference in the United States earlier this year. Unlike his colleagues, the jovial young man lacked typical Japanese reserve and was openly enthusiastic about his work even though he spoke English haltingly.

Then, perhaps tiring of all the questions, the researcher suddenly turned the tables on the reporters. "How many hours a day do you work?" he asked, pointing at each one. "And you? And you? And you?"

The astonished reporters replied that they worked between eight and 12 hours a day, five days a week, and occasionally on weekends.

Our Japanese physicist then said that he left home at eight o'clock in the morning and went home about midnight. Moreover, he kept this up seven days a week with the exception of spending one day a month with his family. Upon hearing this, the reporters all shook their heads and murmured sympathetically.

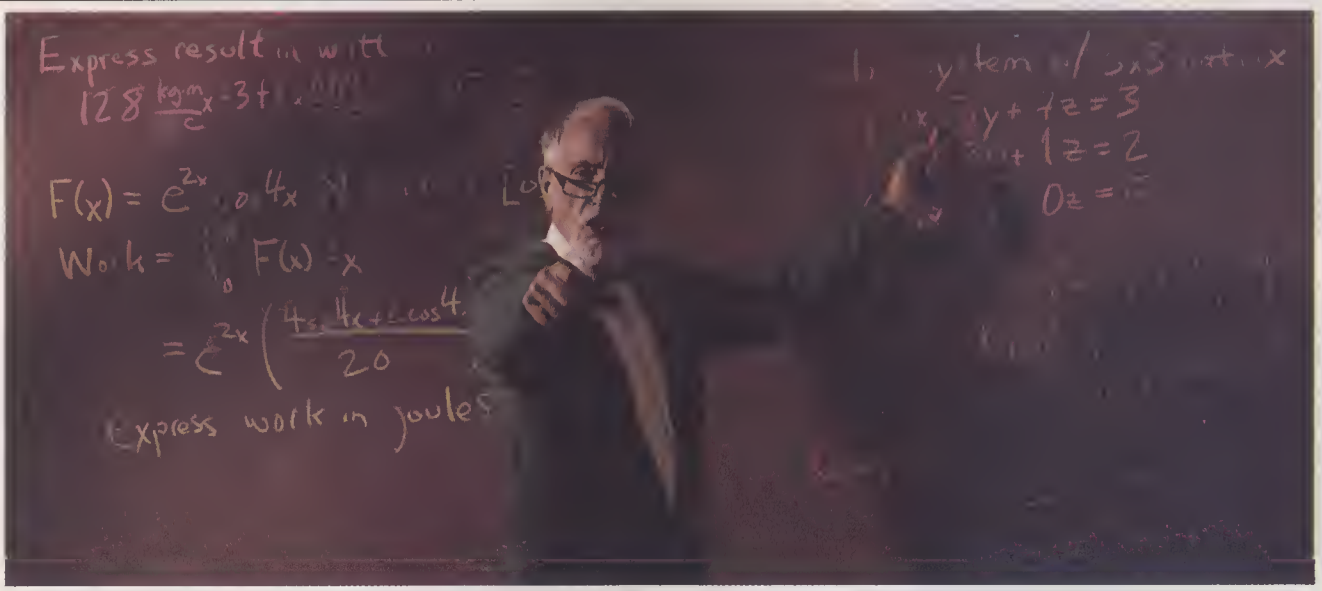
The researcher said his wife recently gave birth to their second child, whom he saw as often as his schedule permitted.

"My baby was 'quantized,'" he said. And, then indicating the length of the baby with his hands, he said, "I saw her when she was this big, then this big, and then this big." Our irrepressible physicist proceeded to inquire about the amount of time the reporters spent commuting to work, how they arranged to care for their children, and whether there were any good shows on Broadway.

The next day, when the researcher presented his paper at a conference session, however, he was all business and all Japanese-style reserve. Perhaps the previous day, the effects of the "water" that his colleague had ordered and that the waiter had misunderstood as "vodka" had had an effect.

Coordinators: Erin E. Murphy, Katherine T. Chen
Consultants: Anne Eisenberg, Polytechnic University; Pamela McCorduck, Columbia University

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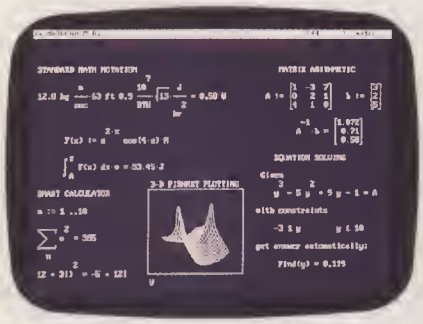


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Putting international patent data to work

Results of a new study should dispel some of the skepticism many industrial managers have toward the usefulness of patent data in technology planning and analysis.

Mary Ellen Mogee, a consultant and researcher based in Great Falls, Va., analyzed statistically two technologies selected from "World Patent Index." This on-line database is published by Derwent Ltd. in Great Britain and is available on Dialog and Orbit. Mogee found it was possible to use the data to:

- Determine the stage of the life cycle a technology is in.
- Distinguish clearly between a mature and an emerging technology.
- Assess how much of the patent activity in a particular technology involves the United States, either as a source of invention or as a market, and how much is going on outside of the U.S. patent system (in general, quite a lot, according to Magee).
- Identify the most active areas of a technology.
- Identify companies doing the most important work, as indicated by how often patents are cited by other patents.
- Identify the technological directions a particular firm is pursuing.
- Recognize whether a firm continues to be active in a technology, has dropped out, or is a new entrant.

(Some of these indicators have been spotted by previous patent studies.) Moreover, after performing her statistical analysis on the two technologies (a mature industrial chemical and the emerging sol-gel technology), Mogee asked experts in the fields to evaluate her findings.

They told her that her conclusions about sol-gel technology conformed "quite well" with their impressions, while the overall picture of the mature chemical conformed "moderately" to "quite well."

Although Mogee's analysis was somewhat less successful in identifying individual firms, inventors, and markets, she told *IEEE Spectrum* that the technique is clearly useful in conjunction with such tools as technology forecasting, and can provide "strong hints" about future trends in a technology and the research directions competitors are pursuing. Mogee also emphasized the importance of using international patent data.

A report of Mogee's findings has been prepared for her sponsor, the Center for Innovation Management Studies at Lehigh University. Copies are available from Mogee at 212 Carrwood Rd., Great Falls, Va. 22066.

Reshaping organizations

The downsizing frenzy of the 1980s has left many organizations with fewer managers to do the same amount of work—and in the same old ways.

These organizations cut staff when they should have restructured the work itself, according to Robert M. Tomasko. Their cost-cutting efforts amounted to little more than "running a vacuum cleaner over the organization chart," the Washington, D.C.-based organizational consultant told a recent executive forum run by Arthur D. Little Inc., of Cambridge, Mass. Today organizations must examine the nature of the work they do and how they can do it better, Tomasko said.

A critical step in this process will be to redesign jobs so that managers manage full-time while others—including former managers—concentrate exclusively on adding value as individual contributors.

Tomasko examined more than 35 companies in the course of research he is doing for *Lean, But Not Mean*, a follow-up to his 1987 book, *Downsizing*. He has found that many middle-management jobs are "mules"—part management and part work better done by individual contributors.

Engineering managers, for example, typically spend 35–70 percent of their time on design work. Another 15–30 percent goes on reviewing reports and other information, and relaying it up and down the organization's communication channels without necessarily adding anything valuable to this information.

To escape this, Tomasko urges:

- A more narrow definition of the job of management, especially middle management. Eliminate anything individual contributors and support people can do. This will lead to fewer managers, flatter organizational pyramids, and greater spans of control.

Although fewer, the managers will be able to spend 80–90 percent of their time, instead of 10–20 percent, as leaders, motivators, trainers, and coaches.

As for the organizational pyramid, even the largest international corporation needs no more than seven to eight management levels. And each manager should receive 20–30 direct reports rather than three to five, while planning horizons should be measured in years, rather than weeks or even days.

- Expand the two-track career ladder to the entire organization, so that all professionals and specialists can choose between a meaningful management career path and an individual contributor one.
- Redesign the organization's information systems to link different functions more effectively and free managers from much of their current information handling.
- Streamline support and control functions, and let more of the functions be done by consultants, contractors, and expert systems.

The organizations that emerge from this kind of rethinking and restructuring will be more innovative, more cost-effective, and more likely to survive the 1990s.

International tech transfer

The globalization of technology puts a premium on a firm's talent for transferring

technical know-how across national boundaries faster and more effectively than its competitors. There is a right and a wrong way of going about this, however.

According to Robert T. Keller and Ravi R. Chinta, the wrong way is simply to rush in to foreign markets. The right way is to begin by recognizing that technology transfer is a process with barriers to the information flow as well as bonds, or bridges, that enhance that flow [*Academy of Management Executives*, vol. 4, no. 1, 1990, pp. 33–43].

Keller is now a professor of management at the University of Houston in Texas, while Chinta is manager of business planning at Sentron Medical Inc., Cincinnati, Ohio. From their study (done while they were at Louisiana State University in Shreveport), it was apparent that successful firms recognize the barriers and bonds peculiar to their situation and develop strategies for dealing with both. Such firms include IBM Corp., NV Philips, and General Electric Co., they said.

Constraints may be imposed by the home or supplier country, as well as by the host or recipient country. Worries about jobs, competition, threats to national security, and "economic imperialism" produce barriers, as do a lack of compatible standards and different cultural values.

Bonds that facilitate technology transfer arise within a company or between or among companies. Bonds within a company can be forged through strategies that create new products and processes or that redeploy existing ones. Each strategy has its variations together with advantages and disadvantages that it is vital to understand.

Bonds between companies include joint ventures, licensing, and even cultural compatibility between firms with similar or shared values; Japan, South Korea, Taiwan, and Hong Kong, in particular, are receptive to transfer of electronics, auto, and steel technology because they value assertiveness and achievement in economic matters.

Keller and Chinta observe that firms can create bonds by choosing the appropriate organizational design strategies and policies for organizational control and human resource management. To give three examples:

- Multinational firms with a global matrix organizational design (in other words, functions in several countries working on one project team) transfer product and process technology across national boundaries more successfully than more decentralized competitors.
- Rotating people through different jobs in different international subsidiaries creates a sense of community.
- Placing manufacturing and sales units in one profit center, even though they are in different countries, creates a bond.

Keller told *Spectrum* he plans to investigate still another means of encouraging international technology transfer: locating a firm's R&D facilities in more than one country. Japanese companies have done this extensively, as have some U.S. firms.

Coordinator: Michael F. Wolff
Consultants: Robert F. Cotellessa, Clarkson University; John Griffin, McKinsey & Co.

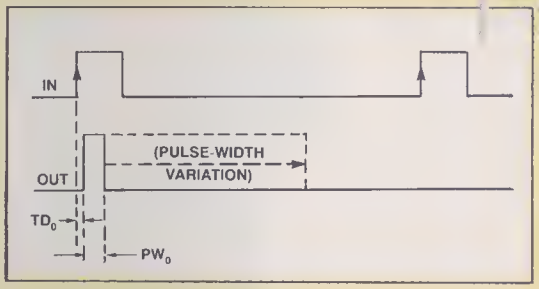
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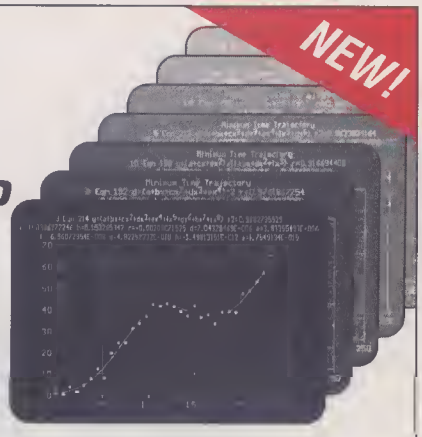
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Open questions on defense

Whenever recession strikes the military/aerospace industries, we worry and wonder whether we can live through the inevitable buffeting with less disruption than we did the last time around.

The challenge is with us again. Can defense programs be reduced to an appropriate level with a minimum of disturbance to the economy and limited trauma to management, professional, and factory personnel? This was one of the questions *IEEE Spectrum* sought to probe when it convened a roundtable of defense and economic experts recently in Washington, D.C. The panel was chaired by Allan C. Schell, chief scientist at Headquarters Air Force Systems Command, and its deliberations are discussed at length in this issue.

The question is one faced not only by the United States, but by other world powers, too. The answer, if you are among the thousands of U.S. employees caught in force reductions, is undoubtedly a resounding "No." The panelists, too, were not optimistic, but rather discussed ways of steering through difficult times—over a period of years—to emerge, one hopes, in reasonably calm waters.

But can this be done in light of the unusually heavy overhead burden borne by the defense industry? In the United States, this has been estimated to represent as much as 30 percent of the value of a contract.

Accounting for a large part of that overhead are the military specifications and procurement regulations. Documentation and maintenance procedures also add to that outlay. Yet, given today's situation, trailer-truckloads of contract documents may need to become a thing of the past. One panelist said that U.S. military companies would have to be taken apart and put together again to be commercially competitive. We often hear the statement today that professional and managerial employees in such companies may not be sufficiently entrepreneurial to survive in the commercial world.

There was a time when military-grade components looked little like their commercial counterparts, being intentionally overdesigned to withstand battlefield environments. This is still frequently the case, particularly for mechanical parts.

But the Department of Defense is moving toward using off-the-shelf electronics, which can be as reliable, or even more reliable, than custom military parts, and orders of magnitude less expensive. The concept of specifying form, fit, and function so that electronic components can be produced using contemporary commercial devices is catching hold. This is in contrast to "build-to-print," in which the technology and configuration of a component is specified.

Form, fit, and function, coupled with just-in-time manufacture, could reduce the costs and logistical complexity of stocking military spares, too.

Unless military and aerospace industries can be made much more efficient, it is unlikely that depressions in military spending can be easily accommodated by adapting managerial and professional talents to commercial products, given the competitive and often cutthroat nature of the latter. But the cost and efficiency gap might be closed, in part, through the simplification of the military procurement process, the use of more commercially built components, the adoption of just-in-time manufacturing procedures, and the application of concurrent engineering techniques to shorten time-to-deployment cycles.

If such should happen, the mobility of engineers and managers between military and nonmilitary projects would be eased, and, one imagines, it would be easier to remobilize those talents for military purposes should the need arise.

Also on the plus side of the conversion equation must be counted the vast resources resident in the 726 government/military laboratories. "They're a gold mine," remarked one of the panel members. But to exploit them for commercial use might require private enterprise to ferret out the technology, license it, and adapt it to commercial needs.

These and other issues are addressed in the special report beginning on page 30.

It's the law

Corporate law, contracts, patent rights, infringements, and litigation have played an important role in the history of the electrical and electronics industries. One need only mention Edison, Westinghouse, deForest, Armstrong, and Sarnoff to trigger a burst of reminiscences about serious, and sometimes bitter, legal disputes. Likewise, company histories are intertwined with machinations involving the law. AT&T, RCA, GE, and IBM come instantly to mind.

Contemporary inventors and recently founded corporations are no less immune from legal concerns. In recent years, the issue of software patentability has added a new layer of complexity to the field.

With this issue we begin a new column that addresses electrotechnology and the law. Called "Legal aspects," the first column is written by Joel Miller (M) of Weil, Gotshal & Manges in New York City. Miller earned his B.S.E.E. from Lafayette College and his J.D. degree from the University of Miami, and is an associate in the firm's technology and proprietary rights group.

The topic, appropriately, is an analysis of the landmark software ruling in the Lotus Development Corp. v. Paperback Software International case.

If you find the column informative and useful, please let us know.

—Donald Christiansen

DEFENSE

HOW MUCH IS ENOUGH?

The Cold War's demise and the decline in U.S. military budgets, coupled with the danger of Third World conflict, as in the Persian Gulf, has created a time of wrenching change for the U.S. defense establishment.

With less money, the country's Armed Services must come to grips with defining the type of fighting force they will have to develop to meet the challenges of the decades ahead. U.S. defense and aerospace companies must now learn how to do business in not only a smaller market, but one whose technical requirements have changed.



IEEE Spectrum examines the turbulent situation in this three-part special report. The military's choices are presented first. Next come the transitional steps being considered by industry [p. 33]. Finally, industry experts weigh the nation's technology options [p. 37].

Toward smaller, more deployable forces, as lethal as can be

When Jerry C. Harrison, a two-star general and aerospace engineers, was put in charge of the U.S. Army's technology base, one of the first things he did was to convene brainstorming sessions in Fort Leavenworth, Kan., and Washington, D.C., to contemplate warfare in 2015.

Because of the thaw between the East and West, Harrison saw a major weapon that he had helped to create— the Pershing IIs— retired early by a 1987 treaty. With the collapse of the Berlin Wall last November, deeper cuts are in progress, except in Harrison's area—technology on which weapons of the next century might be based.

To guide today's lab work, the 48-year-old major general gathered his top technologists and some U.S. field officers from regional hotspots for war gaming last June. Their main conclusion confirmed many experts' basic view: as Harrison put it, his armed service is "going to be smaller, more deployable, and as lethal as we can make it."

Harrison could have been speaking for the U.S. Navy or Air Force as well (or, for that matter, for the Soviet military). Even though superpower enmity, the major impetus for the arms race, is being replaced by cooperation, harnessing the latest technology for a nation's troops will probably remain in vogue as long as the world is perceived as a dangerous place.

Many experts, including U.S. Government officials, urge a vigorous military R&D program but a more selective modernization of items actually deployed. Yet if a military's ultimate aim is to discourage war (and not merely to win the conflicts it is engaged in), introducing potent new weaponry, particularly at lower force levels, could be counterproductive.

To reconcile such apparent differences in a potent but not too potent force is an unfamiliar challenge, but one critical to security if future rounds of arms control talks reduce forces to low levels.

The North Atlantic Treaty Organization (NATO) accounts for perhaps half of the Pentagon budget, according to analysts. Most of its weapons systems were designed to battle Soviet forces in Europe. Authorities like David C. Jones, former chairman of the Joint Chiefs of Staff, believe that "as we get down to it, there is no credible threat of conventional attack" in Europe.

Regarding regional threats, U.S. strategists are as yet undecided what to do, such as how quick a response is needed, notes Ivan Oelrich, a Washington, D.C. defense analyst. In this respect, he said, the Iraqi invasion was timely since it is one of the most stressful regional cases, jeopardizing the West's oil flow. It also reminded the public that a powerful military is still required. But Oelrich and Janne E. Nolan, a senior fellow at The Brookings Institution, Washington, D.C., agreed that in the near future the Third World will become no more threatening or dangerous than in the past. In short, it is no substitute for the diminished Soviet conventional threat.

Strategic revisions

The first U.S. defense budget of the post–Cold War era will be a compromise because the House wants more drastic cuts than the Senate, which wants more drastic cuts than the Administration. Many believe that on the strategic level penetrating bombers, intercontinental ballistic missiles (ICBMs), and lots of carrier battle groups are not as necessary as in the past. On the tactical level, many heavy forces designed for Central European combat are under attack. (The view of a bipartisan 11-member committee including former ex-Reagan Pentagon official Lawrence Korb and former Central Intelligence Agency director William Colby is indicated in the table on p. 32.)

Even with a moderately rising defense budget, it would be difficult to deploy the systems ordered during the Reagan administration buildup. With a constantly dropping budget, funds for procurement could dramatically shrink, since non-discretionary funds like military pensions will make up a greater portion of the smaller total.

The Bush administration, reversing its intention of just a year ago to seek real rises in the Pentagon budget, now plans substantial cuts. Retired General Edward C. Meyer, who lamented the "hollow" Army he inherited as chief of staff in the early 1980s, said that a 25 percent cut over five years is feasible, even with a conservative "insurance policy" to respond to surprises. Other

John A. Adam Senior Associate Editor

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groups, like a bipartisan one assembled by the Defense Budget Project, a private Washington, D.C., group, advocate a 50 percent reduction over 10 years.

Such cuts may alter the way the Pentagon arms its forces. "The defense industry will have to be ready to produce, but not make anything," said Lieutenant Colonel Robert Latiff, a Harvard University National Security Fellow. A vigorous R&D program and the mere potential to build—"shadow deployments"—will be a large factor in future deterrence, agreed Roger Hagengruber, vice president of Sandia National Laboratories, Albuquerque, N.M.

Smaller sales could also mean exorbitant unit costs—but not necessarily. With less money to develop prototypes, advanced simulation will become critical to the evaluation of alternatives early in the R&D cycle and to exploring the leverage of new technologies in war games, according to Eugene Gritton of the Rand Corp., Santa Monica, Calif. New technology might not be tacked hastily onto platforms until its own process engineering is perfected, leading to lower costs and greater reliability of advanced weaponry, Latiff said.

New manned platforms like tanks or aircraft will be rarer. "Subsystems will replace subsystems for upgrades," according to George Millburn, a former Pentagon technology official now at the Aerospace Industries Association of America, Washington, D.C.

Because of the diminished potential for large sales, defense contractors may have less incentive to innovate on their own initiative. Charles M. Herzfeld, the Pentagon's director of research and engineering, acknowledged he was concerned about this, adding it is even more reason for stable Pentagon R&D funds and greater efficiency in DOD laboratories.

Further diffusion of technology worldwide, more integration of military with civilian technology, and slower modernization may make it tougher for "by far the most powerful country on the earth" to keep its technical military edge, said analyst Benoit Morel of Carnegie Mellon University in Pittsburgh. He added that the Pentagon's "management of innovation now is very suboptimal."

Spending large amounts of money to get the last 10 percent of performance may be less critical now that likely future threats are neither as technically sophisticated nor as multifaceted as the Soviets' were, said Matthew Bunn, associate director of the Washington, D.C.–based Arms Control Association.

Sandia's Hagengruber believes, however, that future regional conflicts, where quickly deployed U.S. forces may be outnumbered, will still require qualitative superiority.

That opinion is apparently shared by Pentagon leaders. Herzfeld, the DOD's chief technical officer, told *IEEE Spectrum* in October that the Pentagon will "try to limit the reductions in science and technology as much as we can," but that such reductions would probably occur.

Certain niches of course may expand. Herzfeld is crafting a technology strategy for the 1990s with the help of the Pentagon's Defense Science Board and the services. The top priority will be computing research, including massively parallel machines, communications within and between machines, and high-definition displays. Sensors for improving techniques for finding things will be the second priority, followed by materials research, said Herzfeld. He expects the full report by January.

Trends and wishes

Earlier this year, U.S. defense officials looked ahead 20 years and sketched out 12 goals to direct R&D.

To aid deterrence and maintain military superiority, the Pentagon's "Critical Technologies Plan" of March 1990 urges:

- Worldwide, all-weather forces for limited warfare without the requirement for main operating bases (including a force that is logistically independent for 30 days).
- Tracking of strategically relocatable targets.
- Defense against ballistic missiles of all ranges.
- Affordable space transport.
- Substantial antisubmarine warfare advantages.
- Global command, control, communications, and intelligence (C^3 I) capabilities to include on-demand surveillance of selected geographical areas and real-time information transfer to top authorities.
- Weapon systems that "deny enemy targeting and allow penetration of enemy defenses" by managing signatures and electronic warfare.
- Air defense systems to "overmatch threat systems."
- Brilliant weapons that autonomously acquire, classify, track, and destroy a broad spectrum of targets.
- Reduction of operations and support resource requirements by



U.S. Department of Defense

The US $43 million F-117A aircraft was the first weapon designed mainly to evade detection. The reduced Soviet threat, however, has brought increased scrutiny to bear on the pace at which to acquire new military technology like stealth.

50 percent without impairing combat capability.
- Reduction of manpower for a given military capability by 10 percent or more.
- Enhancement of producibility and availability of future weaponry.

Each service naturally has its own vision. One for the U.S. Army includes a force powered by electricity; robotic tanks and aerial vehicles and bionically enhanced soldiers with embedded chips, the ability to sleep when commanded, and exoskeleton systems allowing individuals to carry 400 pounds (180 kilograms) around the battlefield instead of only 100 pounds (45 kg). "Multispectral smoke" and variable obscurants also are alluring, said Harrison. "You might say, 'Okay, guys, today we're going to shoot No. 49. Tune in your goggles,' to see but not be seen."

The U.S. Air Force, in its Project Forecast II report, offers dozens of initiatives to maintain military supremacy, including "electronic associates" to aid pilots and the possible stationing of robots on the moon. The U.S. Navy, in a report on ship characteristics in the year 2010, discusses everything from easily cleanable toilets "with adequate ventilation" to laser weapons, torpedo-killing drones, and microwave-beam guns.

A post–Cold War emphasis on lighter, more mobile forces means that, aside from advances in weaponry and sensors, training and command-control are critical. Here simulation and computer and communications networks offer great potential. Other safe bets are fuller use of the electromagnetic spectrum (for support and as a weapon) and faster, smarter, more accurate, and more lethal weaponry that further distances humans from the battlefield.

Potential savings from weapons cutbacks

New military system	Bush administration	Korb task force	
		Cutback	Savings, in billions of U.S. dollars
C-17 Cargo Aircraft	Build 120	Cancel	Up to $22
Advanced Tactical Fighter	Build <750	Continue R&D	Up to $62
SSN-21 Submarine	Build 28–30	Cancel	At least $30
Forward Area Air Defense System	Deploy	Continue R&D	Up to $9
Advanced Medium Range Air-to-Air Missile	Deploy	Cancel	Up to $7
Advanced Tactical Aircraft	Build 620+	Continue R&D	Up to $47
LH Light Helicopter	Deploy	Cancel	$41
ATACMS Army Tactical Missile System	Deploy	Cancel	$1
Joint Surveillance Target Acquisition Radar System	Deploy	Continue R&D	Up to $5
SRAM-T Short Range Attack Missile and FOTL Follow-On To Lance	Deploy	Cancel	$2

Source: Task Force of Defense Budget Project and the Committee for National Security (updated from March 1990)

Long-term stability amid change

Coupled with improved C^3I, some believe new generations of easily dispersed weaponry like terminally guided munitions from artillery and non–line-of-sight missiles can make prospects very poor for the massed armor of an attacker.

Paul K. Davis, director of the Rand Strategy Assessment Center, part of a Pentagon think tank, envisions an East-West military stability in which both sides correctly believe that the defender is quite likely to prevail in a war. "The more this is true," he said in a report co-authored by colleague Robert Howe, "the less the pressure for an arms race (unless one nation is determined to be aggressive)."

Each side can maintain security with reasonable defense burdens that are either constant or shrinking, "in significant part because the threats to be balanced are well understood and only slowly changing." The reverse is also true: lack of an arms race contributes to military stability if the current balance favors the defense. Stability would also mean that in the event of invasion the defender would win, and that this situation would be unaffected by moderate changes in forces, such as one side introducing a new generation of tank or having somewhat more troops than it ought, Davis explained.

He called it "potentially quite dangerous" to scale down NATO forces if the Western alliance does not make fundamental changes in force posture, command-control, and operational strategy. He added, "Parity is no panacea," pointing out that many wars have been fought at parity, and the defender has often lost. He suggested that before any pact is signed under the second round of talks of the Conventional Armed Forces in Europe (CFEII), the sides should enhance the stability of an eventual low force level regime by such "operational arms control" measures as: withdrawal of excess artillery ammunition beyond that needed for defense; constraints on high-readiness reserve units; constraints on out-of-area ground forces; and limits on certain types of large-scale exercises.

The two sides could evolve to force postures with a smaller ratio of attack-suitable to defense-suitable weapons and units, while retaining high mobility and flexibility, Davis said. This might be aided by limiting types of mobile air defenses and avoiding severe constraints on transport helicopters, attack helicopters, and thinly armored personnel carriers, since these systems improve the defender's mobility but are extremely vulnerable in the opponent's rear areas. (Non-offensive forces should lack, as a whole, the means for long-distance invasion operations.)

Ex-Pentagon official Millburn also believes that "we have to make the use of force unattractive in the world," but that a strong offense is required to deter attack. Richard Garwin, a military technology analyst and member of the Pentagon's freewheeling Jason panel, said, "A posture which is less offensive is a good idea." However, he is skeptical whether an inability to strike the other side can be maintained.

Even if attainable, Nolan of Brookings believed that to make nonoffensive defenses feasible there must be some level of mutual accommodation, something unlikely in, say, the Middle East.

End game for arms control?

General Jones, acknowledging that the Warsaw Pact is irreversibly dissolved, called for changing the approach to arms control. "End-game" propositions are no longer pipedreams, so the nation should determine a desirable final level for stable, nonintimidating deterrence. This will never be a static because of technical progress, he said, but instead of the military apparatus focusing on force destruction, it could focus on mutual security, and perhaps eventually even change the targeting in Europe.

Due to the Gulf crisis and the new Soviet-U.S. cooperation, "the chance for arms control is better than it has ever been," said Brookings' Nolan. Bunn of the Arms Control Association argued that much deeper cuts in nuclear weapons and attack-suitable conventional forces should be on the table during the next rounds of arms talks. Operational measures of the kind favored by Davis and technological restraints to prohibit destabilizing new weapons should also be included, he said, mentioning antisatellite weapons, maneuvering warheads, and depressed-trajectory ballistic missiles as candidates to be banned.

Cases against unfettered technical development are being heard. Ex-Army chief of staff Meyer told *Spectrum* that some technology is destabilizing even if bilaterally deployed. He cited lasers that can blind optical surveillance, and another weapon, deployable today, that he declined to specify. Noting that it is hard to restrict lab research, he said there may be a way to curtail development of prototypes.

Because much R&D has unforeseeable and multiple missions, only in certain areas (like the ban on biological weapons) would it be desirable to put an *a priori* ban on military research. Sandia's Hagengruber believes that to avoid energizing the arms race, weapons could be assessed before being tested or deployed by their capacity to enhance stability. A similar approach, carried out by an international center, has been recommended by Manfred Müller, a United Nations disarmament advisor and department head of the (former) East German Academy for Political Science, writing in the 1989 book, *Conventional Arms Control and East-West Security*.

Destabilizing qualitative improvements are potentially more serious in the strategic realm. As arsenals get smaller, a disarming first strike becomes more feasible, noted Oelrich. But arms control can limit the so-called counterforce weapons, like certain ICBMs, and leave more benign retaliatory forces, like submarine-launched missiles. The first round of the Strategic Arms Reduction Talks, Start I, will eliminate as much as 30 percent of strategic warheads by the end of the century. Start II negotiations would cut more, indicating that each side would have several thousand warheads.

When each side has less than 3000 warheads, then the strategic defense phased-reduction approach may make sense, some believe. To help diplomacy keep pace with strategic technology, Bunn favors establishing yearly quotas on flight tests of ballistic missiles and a comprehensive ban on nuclear weapons tests. He conceded, however, that a lower threshold on nuclear bomb tests and quotas would be more politically acceptable and verifiable.

The Persian Gulf notwithstanding, some say that invasions are losing their allure. Oerlich noted that occupying conquered territory is difficult nowadays. Kosta Tsipis at the Massachusetts Institute of Technology in Cambridge said that the utility of combat for changing the *status quo* is declining, witness Korea, Vietnam, Afghanistan, and Iran and Iraq.

If alternatives to war become preferable, unilateral disarmament may occur in many countries now spending high portions of their gross national product for the military, said Herbert York director emeritus of the Institute on Global Conflict and Cooperation at the University of California, San Diego. Already, as national security embraces a broader scope than mere military might, the Pentagon is finding itself in nontraditional roles such as fighting drugs and forest fires. The "greening of the Pentagon" is also described in a recent 10-year defense market forecast by the Washington, D.C.–based Electronic Industries Association as one area of opportunity, including work on hazardous wastes, strategic environment research programs, and nuclear production cleanup. To help offset the decline of defense work, MIT's Tsipis believes that the U.S. government should ask its contractors to devise new marketable techniques to monitor and control the global enemy of pollution. National regulations and international pacts could then create a market for the antipollution and energy-efficient technology. Cooperation might be sought with the Soviet bloc.

The United States spent trillions to win the Cold War, notes Brookings' Korb. Now is not the time to be restrictive with technology or grants to the Eastern bloc: "The enemy that we used to think was communism is now chaos," he said. Recalling the enmity of the vanquished toward the victors in the U.S. Civil War and World War I, former Pentagon official Millburn said, "We have to do something" for the Soviet bloc.

To probe further

"Restructuring the US Military," a March 1990 report by a joint task force of The Committee for National Security and The Defense Budget Project, both based in Washington, D.C.; "New Thinking and American Defense Technology," August 1990, by the New York City–based Carnegie Commission on Science, Technology, and Government; and "The Guns Fall Silent," Institute for East-West Security Studies, New York, 1990, are among recent post–Cold War reports. "Conventional Arms Control: The Limits and Their Verification," by Ivan Oelrich (Center for Science and International Affairs, Harvard University, 1990) and "Arms Control's Enduring Worth," by Matthew Bunn, *Foreign Policy*, Summer 1990, also merit study.

The weekly *Aviation Week and Space Technology* and the newsletter *Defense Week* track modernization. The *Bulletin of the Atomic Scientist* in Chicago, and *Arms Control Today*, published by the Washington, D.C.-based Arms Control Association, cover arms control issues.

The U.S. Congressional Office of Technology Assessment is preparing a background paper, due in 1991, on future defense technology and its requisite industrial base.

The March 29, 1990, testimony from the director of the Defense Advanced Research Project's Agency is useful, as is the Pentagon's March 1990 report, "Critical Technologies Plan." The paper "Planning for Long-Term Security in Central Europe" by Paul K. Davis and Robert D. Howe of the RAND Corp., Santa Monica, Calif. (202-429-4600), should be available by December. ◆

Suppliers are challenged to downsize gracefully as they seek to diversify

As August gave way to September, weapons, fighting machines, electronics, and surveillance gear poured into the Persian Gulf region at a rate not seen since World War II. Swarms of officials and journalists from all over the world scrutinized the materiel for clues to military advantages, capabilities, and intentions, and the unfolding crisis soon became as ironic as it was tense. The companies that produced the systems were for the most part laying off workers, trimming their operations, and looking for nonmilitary business opportunities.

Such inconsistencies have become part of day-to-day operations for many North American, European, and Japanese defense firms. In those regions, planned defense budgets will soon either reduce military spending significantly below current levels, or, as in Japan, cut back planned increases in defense spending.

In the United States, for example, Secretary of Defense Dick Cheney has requested nearly US $78 billion to procure military systems in 1991, more than 9 percent below the 1990 budget for procurement, after inflation. Cheney requested just over US $38 billion for research, development, test, and evaluation (RDT&E), a decrease of 0.9 percent from the 1990 level.

The actual reductions imposed will in all probability be even steeper than those suggested by Secretary Cheney, since the U.S. Senate and House of Representatives have both proposed lower figures for procurement and RDT&E. According to Congressional sources, the Senate recommended US $67.4 billion for procurement and US $36.5 billion for RDT&E; the corresponding House figures were US $63.95 billion and US $34.8 billion. At press time, Senate and House members were in conference over compromise figures, as part of the extraordinarily intense negotiations over the 1991 fiscal year budget.

Defense companies hoping to offset the anticipated decline in U.S. sales by selling to European armed forces are likely to be disappointed. Most European nations are now planning to reduce defense spending by proportions similar to, or greater than, those planned in the United States.

But the Mideast military buildup, in response to Iraq's invasion of Kuwait last August, has added a perplexing twist to what most observers had expected to be another relatively straightforward military drawdown. Many top defense executives contacted by *IEEE Spectrum* early during the Mideast crisis were quick to cite the Iraqi action as the kind of tactical military situation that Western nations increasingly need to be prepared for, but that had received little attention during the decades-long Cold War.

Glenn Zorpette Associate Editor



Martin Marietta Information Systems Group

The U.S. Federal Aviation Administration's ongoing multibillion-dollar effort to upgrade air-traffic-control and weather-tracking equipment at major airports is providing business for many defense-oriented firms.

"The threats are shifting from Europe to the developing world," said Willam Bardo, technical director of GEC-Marconi Ltd. in Stanmore, Middlesex, one of the largest European defense firms. "All of the Western nations are in a state of flux over this."

"Iraq is theoretically a Third World country, but they've got a million troops, MiG 29s, and some of the best tanks [Soviet T-72s] in the world," added Robert G. Morra, vice president-technical operations at Martin Marietta Corp. in Bethesda, Md. "How far has peace really broken out?"

In the United States, several defense firms have already benefited—or are expected to as soon as the Government approves sales of aircraft, weaponry, and air-defense systems to its Mideast allies, particularly Saudi Arabia. McDonnell Douglas Corp., for example, was given approval in early September to sell 24 F-15 fighter aircraft to the Saudis. The massive U.S. airlift of troops and equipment to the region could also bolster the St. Louis, Mo., firm's C-17 transport plane project, which had been plagued by schedule and cost overruns and had been severely cut back by Cheney.

All told, the Bush administration was considering allowing the sale of some US $21 billion worth of military systems, including some relatively advanced ones, to the Saudis. This package would include dozens or hundreds of helicopters, trucks, tanks, missiles, rocket launchers, and other armaments. In mid-October, however, Administration officials were reportedly planning to pare down the package to appease members of Congress who were alarmed over the possibility that the advanced weaponry could in the future fall into the wrong hands and be used against U.S. or Israeli forces.

Strategies vary

Despite scattered reports of such sales and the prospect of more, depending on developments in the Gulf, most defense executives doubt that the windfall will amount to more than a brief reversal of an otherwise downward economic trend. The Gulf crisis "has certainly perturbed the system," said Henry L. Bachman, vice president of engineering at Hazeltine Corp. in Greenlawn, N.Y. "But I think in the long term it is not going to change the thrust of the Defense Department's plans to consolidate."

Defense contractors apparently agree; most have formulated far-reaching strategies to cope with the downturn, starting with staff reductions. Virtually all major defense firms have begun laying off workers or have announced plans to do so. In one of the most significant recent announcements, the Groton, Conn.–based Electric Boat Division of General Dynamics Corp., maker of the Navy's Los Angeles–class and Trident submarines, said in September it would dismiss 1000 workers by the end of the year. The company predicted that layoffs could reach 4500, or half of its total workforce, by 1995. Just about all of southern California's aerospace giants, including Lockheed Corp., Hughes Corp., Northrop Corp., and Rockwell International Corp., have also announced major staff reductions [see "Reemployment assistance," *Spectrum*, November 1989, p. 52].

In addition to these reductions, many defense companies plan to diversify into, or expand their share of, nondefense work and contracting. Others, notably General Dynamics and Northrop, do not. "We are concentrating on transitioning important projects, like the B-2, into production," explained Northrop spokesperson Sally Koris.

Defense analysts and executives, including those seeking nondefense business, have few illusions about the difficulties defense firms face in competing outside their traditional markets. "A lot of defense contractors have tried to diversify, more often than not without a lot of success," Bachman noted.

During the defense industry decline after the Vietnam War, many U.S. defense contractors tried to enter commercial markets. Rolm Systems in Santa Clara, Calif., now owned by Siemens AG, began as a maker of rugged military computers but transformed itself into the United States' third largest producer of private branch exchanges (PBXs). However, more typical experiences were those of Boeing's Vertol division near Philadelphia and the Grumman Corp. in Bethpage, N.Y.

Both made ill-fated forays into the transportation business, Boeing by manufacturing light-rail cars, and Grumman by purchasing the Flxible Bus Co. of Delaware, Ohio (acquisition of a nondefense firm remains a popular method of entering commercial markets). Boeing's rail cars were put to use in Boston, where they were so unreliable at first that the Massachusetts Bay Transportation Authority and others filed lawsuits, leading to Boeing's exit from the business. Grumman sold the bus company just five years after buying it in 1977.

Studies over the years have identified numerous reasons for this dismal record. A recent report by the Washington, D.C.–based National Commission for Economic Conversion and Disarmament, a nonprofit educational organization, noted that "military technology is increasingly applied and specific in character to military needs" and thus of "limited use for civilian markets."

Also troublesome is the entrenched culture at large defense firms, where products are typically built under sole-source contracts. The need to achieve unusual performance or high reliability under extreme environmental conditions, relative to those of commercial products, often results in relatively high cost.

Another problem, observed Al Frascella, a spokesman for TRW Inc.'s Systems Integration Group in Fairfax, Va., is that defense companies have relatively high fixed expenses, which support the extensive paperwork that surrounds Government contracts. Such overhead makes it difficult or impossible to compete with commercial firms, and can make it necessary for a company to spin off a separate subsidiary without the overhead to perform all but major jobs.

Finally, defense firms are also hindered in commercial markets by a lack of distribution networks, service organizations, and brand recognition. "Market positions are earned by years of servicing markets, developing and expanding niches based on understanding requirements, tastes, and the other factors that shape consumer preferences," said Weyman B. ("Sandy") Jones, vice president of public affairs at Grumman. "The notion that just because a company can make something it can make a business of it is naive, but this notion underlies the talk—and proposed legislation—for conversion."

Lessons learned

Defense executives planning to diversify are doing so with the past very much in mind, and with far more caution than in the mid-1970s. "This time around, many of the aerospace companies remember that diversification was a lot tougher than had been anticipated," said Miriam Reed, a spokesperson for Grumman. "They're sticking a lot closer to the things they know something about."

One of those things is dealing with the Government. When the Bureau of Land Management in the U.S. Department of Interior decided recently that it needed a computer-based system to automate its land records, it soon found that it could choose from among several of the country's top defense contractors to build the system. Although a formal request for proposal (RFP) has not yet been released, TRW, Martin Marietta, Hughes, and other defense firms have expressed interest in the project, called Almars (Automated Land and Mineral Record System).

The U.S. Postal Service, which is trying to automate by 1995, also stands to benefit. Martin Marietta has won two contracts totaling US $190 million to build machines to sort bar-coded letters at a rate of 36 000 pieces per hour and large envelopes and periodicals at 10 000 per hour. A third contract, not yet awarded, is for systems to sort mail into an order corresponding to letter carriers' routes.

The rub, according to one contractor who asked not to be identified, is that many nontechnical Government agencies, such as Land Management and Housing and Urban Development, are unaccustomed to asking for technical proposals. Testimony before the House Government Operations Subcommittee on Agriculture last Sept. 18 revealed that the Department of Agriculture had paid almost US $62 million for a computer system that was originally projected to cost US $7 million. The contractor, Arthur Andersen & Co., Chicago, blamed the discrepancy on instructions it had received from the Agriculture Department, which the company called "vague."

"Many nondefense agencies don't really know what it is they want to do," *Spectrum*'s source said. "They're not as specific. They don't know what's out there. So their RFPs tend to be vague. It makes it tough to estimate price," said the source, who has dealt with Government agencies both inside and outside the defense establishment.

Other nondefense Government agencies—notably the Federal Aviation Administration (FAA) and the National Aeronautics and Space Administration (NASA)—are somewhat more at home with technical proposals. Many defense-oriented firms are already participating in NASA's space station project, and are hoping for a role in the proposed manned voyage to Mars. They anticipate other opportunities in connection with the wide-ranging Mission to Planet Earth, a planned deployment of a series of earth-observation satellites and sensors.

The FAA, which in 1981 initiated a US $15.8 billion, nationwide upgrade of weather and air-traffic systems at U.S. airports, has been a major source of nondefense income for a number of contractors, including Martin Marietta, TRW's Space and Defense Sector, and Norden Systems, the Norwalk, Conn.–based defense electronics and radar subsidiary of United Technologies Corp. Under a series of contracts worth about US $800 million, Martin Marietta is serving as overall system engineer and integrator for the FAA plan, now known as the Capital Investment Plan. Marietta has also won smaller contracts for similar work in Canada, France, and Australia.

Many of the roughly 90 major programs in the Capital Investment Plan involve radar technology. Earlier this year, Norden installed the first of a series of radar-based systems for monitoring activity on runways at Greater Pittsburgh International Airport. The systems evolved from Naval radar technology developed by Norden for search and navigation.

Another 29 of these Airport Surface Detection Equipment systems are scheduled to be installed at U.S. airports over the next several years under a US $100 million FAA contract. Norden recently won a follow-on contract to add automatic collision-avoidance systems, which will sound alarms in the control tower when aircraft or airport vehicles come too close to one another on runways.

One of the largest FAA projects is the multibillion-dollar Advanced Automation System, the next-generation air traffic control system being built by IBM Corp. TRW's Systems Integration Group is also working under contract, advising the FAA, evaluating IBM's work, and performing related tasks, such as writing and testing software. TRW has also moved aggressively into the security field, providing the New York Stock Exchange with a computer-based system that controls access to the building and various parts of the exchange, such as the trading floor and observation galleries. The company hopes to sell similar systems to operators of embassies and airports (it is now doing studies for an airport in Japan), according to Frascella.

System recognizes speaker in four seconds

Relatively small defense firms are also looking for nonmilitary contracts. Electronic Warfare Associates, a privately held Vienna, Va., firm founded in 1977, has developed a crisis management system that it hopes to sell to the FAA, the Federal Bureau of Investigation, and others. The system allows agents coping with a crisis—a hijacking, bank robbery, or hostage situation, for example—to enter relevant data as it unfolds into an IBM PC AT computer.

As the data are entered, a record of the event is created, with all developments logged with the time they took place. After the crisis, the entire record can be archived to a floppy disk and stored for future use, during a court trial or an internal investigation, for example. The company recently developed a portable command center for the system that fits in three large briefcases.

Another system for which the company has high hopes is a PC-based language- and speaker-recognition system. Based on a Texas Instruments TMS320C30 digital signal-processing chip, the system can recognize a human voice in 2 to 4 seconds after recording and analyzing a 30–60-second sample of that voice, according to program manager Richard B. Friedel. The system identifies the most common phonemes and other speech characteristics, and works independently of the words and language spoken. The latter feature is important when the subject is uncooperative, Friedel noted. The voice may be live, recorded, or transmitted by telephone or radio, he added.

Although the US $35 000 system was originally developed for military and intelligence agencies, Friedel is trying to market it for applications in telecommunications, security, and law enforcement. The first buyers of the system are two Canadian Government agencies, he reported.

Another recently formed commercial venture will offer diverse applications of bar-coding for use in factories, warehouses, transportation facilities, and the like. The company has also just

Zorpette—Suppliers are challenged to downsize gracefully as they seek to diversify

opened a factory in Beckley, W. Va., to manufacture printed-circuit boards with surface- or conventionally mounted ICs; although oriented to Government work, the company will actively seek commercial users, Friedel said. Norden, too, is seeking commercial users for its military-developed surface-mounting and robotic component-placement technologies, a spokesman said.

Two phases

Electronic Warfare Associates' two-phase approach—seeking nonmilitary contracts first and then nongovernment, commercial work—is a common strategy. Indeed, the ability of defense firms to succeed in nongovernment markets is increasingly regarded as healthy from a corporate as well as national standpoint.

To some observers, the alleged decline of U.S. national competitiveness can be accounted for partly by the fact that a vast number—about a third, by most estimates—of the country's engineers and technical workers have defense-related jobs that do not directly advance national competitiveness. These observers say that the United States must use the current period of reduced tension between the superpowers to repair its infrastructures and redirect more of its technical talent to advancing technologies critical to competitiveness.

"I am calling for a serious conversion to civilian production," said Seymour Melman, professor emeritus of industrial engineering at Columbia University in New York City and chairman of the National Commission for Economic Conversion and Disarmament. "What's going on around here is a continuing decay in the capacity for production in the main capital-goods producing industries [heavy-equipment, machinery, and so on]. That kind of production isn't replaced by a mission to Mars."

However, the scarcity of successful commercial products derived from military technology and produced by defense-oriented firms seems to indicate the difficulty of such a transition. To the surprise of some defense executives, commercial success often depends almost solely on factors like marketing, manufacturing, and customer service, rather than technical prowess or R&D.



Martin Marietta Information Systems Group

Martin Marietta technicians test a prototype mail-sorting system built for the U.S. Postal Service. Under a US $138 million contract, the Bethesda, Md.-based company is building 614 of the machines, which sort bar-coded mail.

One of the more impressive recent successes is GEC-Marconi's direct-broadcast by satellite (DBS) business, which makes antennas and low-noise converters for home reception of satellite-television signals. The company's product is based on its military-derived microwave radio technologies. In less than three years, GEC-Marconi has become the world's largest supplier of antennas for DBS reception, producing 50 000 per week.

Len Ogier, assistant managing director of Marconi Defense Systems Ltd. and head of GEC-Marconi's civil microwave business, told *Spectrum* that one of the most critical challenges was "acclimatizing ourselves to the business and adapting to a commercial environment." Compared to its military projects, he added, the technology involved was "fairly conventional."

The company's interest in the market began with the launching of two European DBS satellites in the late 1980s. At that time no European companies were producing DBS antennas in high volume, but many companies were doing so in Japan, Taiwan, Korea, and the United States. GEC-Marconi began a preliminary development program, and received its first orders one Friday afternoon in the summer of 1988. By the following Monday, Ogier recalled, a team had been set up consisting of design, purchasing, and product specialists. "We just cleared an area and put those people in it and set up a business," he reported.

Recognizing the company's capabilities—and limitations—was important. "Where we believed we had the expertise, we made use of it. But we were not too proud to use the expertise of other companies that had something to contribute, particularly in the area of volume production." An auto-parts firm, for example, was tapped to manufacture some of the antenna's components. But GEC-Marconi engineers designed the antennas and all circuitry, winning a few patents in the process. "They actually saw their products being used, and it was a great boost to them," Ogier said. "They got personally involved when something went wrong." All of the engineers were accustomed to working on defense systems that they rarely saw after the systems were deployed.

The company also needed a larger sales, marketing, and customer service operation. Since many buyers had their own money at stake, a higher level of responsiveness was required than is standard in military contracting, where sales are typically governed by competitive bidding, personal relations, or politics.

Emboldened by the success of its DBS business, GEC-Marconi is now considering many other commercial possibilities, Ogier said, none of which have been made public. Before the company will commit significant funds to a venture, it performs a business assessment, identifies applicable technologies, and then outlines a plan. "Frankly, not many make it to that stage," Ogier said. "We've got to believe we've got something important to offer, such as breadth of systems understanding, or a specific technical area we can apply. Overall, the systems understanding has been a benefit in terms of making proposals. We can not only sell the product, but we can also support the complete system in which we sell the product."

This systems competence is a strength that can set a defense contractor apart from competitors more at home in the commercial world, Ogier added. GEC-Marconi recently built a multichannel video system to redistribute DBS signals from a central hub throughout a residential area. One reason why the company won the contract, Ogier theorizes, is that it considered tradeoffs in the entire system, and was able to explain and make a persuasive case to the customer for each tradeoff.

TRW spokesman Frascella agreed, adding, "You won't find a TRW trying to make airplanes, but you may find an airplane company trying to do what we're doing [systems integration].

"There are lots of commercial jobs out there," he concluded. "You just have to find the niche where you fit best." ◆

Expert observers: defining national technology options

To gain further insight into the problems with which reduced Federal budgeting confronts the U.S. Department of Defense (DOD), IEEE Spectrum *asked industry executives to discuss the situation as candidly as possible. The following article presents the highlights of a meeting that took place in Washington, D.C., in mid-September.*

Taking part in the discussion were:

Robert S. Cooper, president of Atlantic Aerospace Electronics Corp., Greenbelt, Md., former head of the National Aeronautics and Space Administration's Goddard Space Flight Center, former director of the Defense Advanced Research Projects Agency;

D. Bruce Merrifield, a consultant to the American Electronics Association in Washington, D.C., former assistant secretary of commerce for productivity, technology, and innovation, and Walter C. Bladstrom professor of management at the Wharton School of Business, University of Pennsylvania, Philadelphia;

David Mowery, associate professor in the business and public policy group of the Walter A. Haas School of Business, University of California at Berkeley;

Allan C. Schell, chief scientist, Air Force Systems Command, Andrews Air Force Base, Md., who asked the questions and helped set the agenda.

Also contributing their views following the discussion were:

George Heilmeier, senior vice president and chief technical officer, Texas Instruments Inc., Dallas;

Malcolm R. Currie, chairman of the board and chief executive officer of Hughes Aircraft;

Alex Mintz, Cullen/McFadden professor of political economy at Texas A&M University, College Station, Texas.

SCHELL: In the early 1970s, when the aerospace industry went into recession, we saw numerous attempts of companies converting to civilian technologies, many of which were unsuccessful. What is the response of industry today to defense budget cutbacks?

COOPER: The CEOs [chief executive officers] I've been in contact with don't believe the Government is taking a responsible position in helping direct what happens to the defense industry. Government is taking pretty much a *laissez faire* attitude and letting the chips fall where they will.

That's a problem for people in [the aerospace] industry because they really would like to know that there's an intellectual force guiding what will be happening over the next 5–10 years. No direction is coming out of the Pentagon or the White House.

For example, the defense budget this year was not in any way hooked onto the geopolitical forces at work in the world. It was just more of the same, and it was restructured only after it was delivered to Congress. People in the industry know that there are major problems coming, and they believe that in many ways they're being hung out to dry.

MERRIFIELD: I hope to see leadership coming out of Darpa [Defense Advanced Research Projects Agency] more than from anyplace else, particularly for next-generation systems. It was a terrible shame to lose Craig Fields [former head of Darpa and now president of the Microelectronics and Computer Technology Corp. consortium in Austin, Texas]. But quietly, I think, Darpa is continuing to set a direction.

There's been such a backlash with Craig's loss that maybe we [in industry] have more freedom than we realize. Perhaps we should take the initiative to work with Darpa to begin to structure a strategy.

The aerospace industry has, of course, been at the leading edge of almost every advanced technology. It has been driving materials, electronics, everything. These areas have been essential not just for aerospace, but for the whole U.S. economy.

The key point is to keep an eye on what is coming down the road. New high-temperature superconductors could revolutionize a lot of things. By the end of the decade, we're going to see electric vehicles begin to challenge the internal combustion engine.

We should try to get a dialog between industry and various elements of the bureaucracy, not only Defense but the Commerce Department, too. We should have a coalition of agencies really behind the technologies that are important to the nation.

It will take private sector initiatives to do that. That's one of industry's failures—we haven't taken the initiative. We should develop task forces around certain areas with the objective of strategic intervention in Commerce and Defense operations.

Consolidation to come

MOWERY: On the civilian side, the airframe industry has become internationalized. Are the major defense contractors moving into more of a risk-sharing subcontracting relationship, or considering it, with U.S. airframe makers, [Europe's] Airbus, and Japanese consortia?

COOPER: There is a lot of interaction both here and abroad. The leading aerospace companies make parts of one another's airplanes. I think there will be a very big consolidation of the major military airplane makers over the next 5–10 years, as well as other consolidations in the defense industry.

What will happen depends, of course, on the defense budget. It could go to about two-thirds to three-quarters of its current US $300 billion in outlays and level off there over one five-year defense plan cycle. Or, the peace dividend people on Capitol Hill could take it down to US $150 billion a year.

But a large fraction of the defense budget goes for nondiscre-

Defense vs. commercial industrial sectors

(a) Contrasts in infrastructures		
	Defense	**Commercial**
Personnel	Large ratio of technical to nontechnical people	Fewer technical people
Customers	Few	Many diverse
Marketing/sales	Dominated by technical people	More balanced
Contracts	Large, long-term	Many customers, orders
Focus	Proposals, documentation	Spec sheets, instruction manuals, warranties
(b) Contrasts in system design		
	Defense	**Commercial**
Requirements	Set by customer	Customer/supplier dialog—specs
System use	Perceived threat	Clear utility
Development cycle	Very long	Medium
Design approach	Revolutionary	Evolutionary
Development cost	High unit cost	Low unit cost
Technology	Advanced	Proven
Product failure	Life-threatening	Inconvenience
Product environment	Harsh/uncertain	Predictable
(c) Contrasts in production		
	Defense	**Commercial**
Qualification	Rigorous	Functional
Differentiation	Customize	Standardize
Lot size	Small	Very large
Maintenance	Skilled	Flexible
Critical concern	Reliability	Cost
Scheduling	Weak	Just-in-time

Alfred Rosenblatt Technical Editor

tionary items like retirement pay. A US $150 billion budget works out to probably US $100 billion a year for maintenance of forces, R&D, and procurement. That would virtually disarm the nation in a very short time.

I don't see that happening. We'll have substantial reductions down to yearly outlays of US $200–$225 billion. We'll maintain our strategic forces at a level to continue deterrence against major nuclear powers, and we'll restructure our land and sea forces to have the mobility to respond to regional crises around the world.

Given that, I see major restructuring of aerospace organizations of 10 000 employees and US $1 billion in sales. I am most concerned about what will happen to small companies like mine, with 100 folks up to maybe a few thousand. These companies make most of the major innovations in defense electronics and aerospace technologies. They are also the ones that determine the long-range future by creating new options and opportunities.



Marvin T. Jones (photos)

Allan C. Schell: ***From the standpoint of surveillance and intelligence, it is no longer just knowing what the Soviets have. It is knowing who sold what to whom and when, and where is it now.***

The Government should strongly interact with the major aerospace companies and help them restructure so there are no great dislocations and personnel problems. We must not waste the resources represented by all that brain power. Perhaps the best thing is to provide individual worker support programs, retraining, relocation, and things of that sort, and let the industry shake itself out.

MINTZ: Actually, during the period of decline in military spending after the Vietnam war, U.S. foreign military sales took up some of the slack. Sales of older-generation equipment grew in the mid-seventies from US $1.5 billion to US $14 billion annually. That substitution effect is evident now in sales to Saudi Arabia. Even if there are severe cuts in the defense budget, foreign military sales are likely to ameliorate their impact.

Another factor now is that the dependence of most companies on defense spending is not as severe in terms of the proportion of their sales as it was in the early seventies. Although the impact on certain companies will be substantial, the effect on the economy in general will not be immediate, and it will also not be direct. In other words, spending cutbacks will have a greater influence on other economic elements—such as investment—and these will affect the future growth of the economy.

It could have been worse for the defense industry. A proposal by the Brookings Institution [Washington, D.C.], for example, recommended even deeper cuts in military spending than Congress wanted.

The situation in the Middle East and Eastern Europe means there has to be some change in the DOD's distribution of resources. There will be new emphasis on logistics, antimissile and antiaircraft, and verification systems, and less emphasis on SDI and big ticket items such as the B-2 Stealth bomber. Politically sensitive systems (such as the V-22 *Osprey*) are likely to be protected by Congress despite the Defense Department's attempts to kill the project.

MOWERY: The U.S. Federal government, almost alone among industrial countries, provides little assistance to individual workers for restructuring. Historically, we've helped "trade-impacted industries" and almost nothing else except for the Job Training Partnership Act. For defense, autos, the steel industry, there's been very little strategic, well-planned assistance.

The interesting possibility exists of an increase in foreign acquisitions of U.S. companies, particularly of second-tier firms and even of one or two at the prime contractor level. A committee does exist—the Committee on Foreign Investment [an interagency government committee chaired by the Secretary of the Treasury]—with power to review such acquisitions. But there is no consistent set of criteria nor any larger framework within which to evaluate these acquisitions.

MERRIFIELD: The real problem is making sure we mobilize our capabilities, and we're not. Consortia must be formed because the multiple skills and resources necessary for the next generation's developments are beyond even a big company—not even an IBM or a General Electric can go it alone.

It's important that we put together collaborative efforts and pool resources and skills. We've gotten over a major hump with the Federal government refusing to set an industrial policy. Now, as long as cooperation among companies is precompetitive and generic, it's OK. That includes anything, really.

Our best model so far is Sematech [the semiconductor manufacturing technology consortium of industrial companies in Austin, Texas, to which the Federal government contributes US $100 million a year]. That's basically the first time we've funded anything from the Government side that isn't managed and directed by the Government. It's all handled by the private sector.

The key to consortia management is to set them up as legal entities with a chief executive officer and a management staff, and the participating companies as limited partners. The partners are protected from antitrust and liability actions and, by law, are not allowed to micromanage day-to-day operations. They set the general charter and objectives and provide the funds.

You don't have to limit the funding to companies. You can have passive investors, pension funds, venture-capital people, and syndicated groups of individuals. If we had set up U.S. Memories [the industry-government consortium proposed last year for making semiconductor RAMs] that way, it would have flown. There are always leading-edge people willing to do new things and take risks. We must ferret them out and work with them to set up models for operating this way.

Conversion to commercial programs

SCHELL: If the defense procurement budget declines between 25–50 percent over the next few years, are we going to see those industries simply decline by that amount? To what degree are they going to convert and be successful on the commercial side?

MERRIFIELD: In the near term, there will undoubtedly be a decline. In the longer term, conversion could be very productive. But it takes three to five years to generate new commercial opportunities, which is why we must consider as many as possible and speed their development. We must realize that wealth can no longer be measured in ownership of fixed physical assets that will be obsolete in three to five years. Wealth will be measured in terms of ownership of, and access to, knowledge-intensive, value-added, technology-driven systems.

You don't care where a good idea comes from. You need to mobilize your resources in concert with whoever comes up with those ideas, telescope the time of development, and get into the marketplace quickly. Historically, we have unprecedented opportunities to do that. But we're not organized for it.

COOPER: There would be problems in shifting to commercial purposes the people and assets as they now exist in the aerospace industry serving the Defense Department. The waste from its management system would automatically produce a 30 percent overhead burden that wouldn't allow them to be competitive.

Those organizations must rapidly teach themselves a new way to manage, and somehow restructure and retrain their workforce, including their engineers. Many skills for dealing with the procurement and acquisition systems of the Defense Department are inappropriate to general business.

Retraining is a serious problem. This has largely been a captive industry. The Government has kept relationships at arm's length. The few percentage points of profit allowed has kept it from being essentially a nationalized industry.

MOWERY: Labor force adjustment problems could be more acute for white collar and middle management employees of some of the large firms, particularly airframe makers, than for skilled blue-collar workers. These large defense firms are not the entrepreneurial, quick-starting firms that we associate with the exploitation of technological and scientific breakthroughs.

It's easy to be pessimistic about conversion to new nondefense lines of business. That is one reason why teaming arrangements between defense and more entrepreneurial firms may be a good idea—it could infect the defense firms with different habits.

Capital in short supply

COOPER: The defense industry offers opportunities, including near-term ones, because a great deal of advanced technology is sort of stuck in there. It has never been allowed to leak out, even though national policy has been to encourage the transition into commercial products and companies. There's still a bureaucratic tendency to protect it, and not to nurture the kinds of relationships with commercial industry that could promote transfer.

Also, right now the defense industry as a whole is in terrible financial shape because it made tremendous investments required by the Defense Department since the early 1980s. It cannot raise capital to any extent to promote new ideas or interests. We have a serious problem with capital formation to support joint ventures at even a minuscule level.

MERRIFIELD: You really put your finger on the problem: the cost of capital. A friend of mine at Toyota tells me that it just borrowed US $8 billion at 1.5 percent from its *keiretsu* banks. Inflation is 3 percent over there so that's a negative cost of capital. In nominal terms, Japan charges maybe 0 percent for zero-risk investments. And it goes up to just 4 percent for high-risk, early-stage developments.

Our real capital cost is 6–8 percent, artificially propped up by the Federal Reserve. We start with 12–14 percent, and it goes out of sight by the time you get to early-stage, higher-risk, longer-term investments. We're really starving for investment capital for next-generation systems.

What we should do is redefine tax incentives for productivity—improving things like re-skilling, R&D, new technology, automation, and innovation. Innovate, automate, or evaporate—that's the rubric. But what we have done by our cost of capital is selectively penalize investments for innovation, automation, and re-skilling.

SCHELL: What Government policies do you see for defense restructuring for commercial activities? Or is that strictly for commercial companies to do?

MERRIFIELD: There is no initiative for this in Government. In part, the attitude is that the only thing you can do is make mistakes; do nothing and you won't make any.

Industry associations are an important element that can bring out a consensus and then hammer away at Government agencies and say, "Wake up, you guys. You've got to get on board with what we have to do." It must be a persistent, repetitive effort.

COOPER: Isn't there some Government policy change, though, that would make it easier for aerospace companies to use some of the technology they've generated over the years to create new products in the commercial sector?

MERRIFIELD: It took a while, but we now have technology transfer laws. Any company that does Federally funded technology owns the exclusive commercial rights and can develop it. For the first time, the technology and all benefits go to them instead of into the Federal treasury.

We have 700 Government laboratories—200 or 300 major ones—developing next-generation systems, but they don't know what they have. It's an absolute gold mine, though, that will take private sector initiative to go in, dig out the technology, get exclusive licenses, and develop it.

Each Government laboratory needs to have a professional function that can ferret things out, make sure they get patented effectively, and then license the right companies to develop them. Trying to get that sort of initiative in the labs is like pulling teeth.

Dual-use technology

SCHELL: I'd like to change the subject to dual-use technology. How should the DOD increase its use of commercial products?

HEILMEIER: There needs to be much closer harmony and integration between the defense and commercial industrial bases. The DOD can no longer afford to maintain its own separate technology base. It must depend on, and leverage, the commercial industrial base more heavily than at any time in the past 50 years.

The barrier to closer integration is not technology, it is DOD's business practices. These have fostered striking contrasts between the currently separate domains. Engineers and companies wishing to participate successfully in the more integrated environment that is inevitable must recognize and adapt to the differences between today's defense and commercial worlds.

For example, success factors in commercial business often include:

- High value to the customer relative to cost.
- Short installation time and low installation labor content.
- Proprietary products.
- Frequent product upgrades and product families.
- Capable manufacturing/flexible manufacturing.
- Service and support.

These stand in sharp contrast to success factors in today's defense sector, which often include:

- Being a member of "The Club"—that is, the group that understands the DOD's byzantine business practices.

Robert S. Cooper: *There's a problem for people in [the aerospace] industry because they really would like to know that there's an intellectual force guiding what will be happening over the next 5–10 years. No direction is coming from the Pentagon or White House.*



- Being first and early in new programs.
- Becoming a partner-in-technology.
- Customized products.
- Specmanship.
- High reliability.

There are other contrasts—in the basic infrastructures and approaches to systems design and production—that also call for adaptation [see table].

In the world in which we now live, the DOD will have to "live off the land." It can no longer afford its own separate industrial base in almost every area.

Some areas will remain uniquely defense. Those who succeed in the new integrated environment will be those who recognize the contrasts between the sectors and adapt their business practices accordingly.

But the burden is on the defense industry people to fit in—not vice versa. To explore new directions means taking risks. Not to do so means taking even bigger risks.

Getting more from other countries

MOWERY: There's a dilemma here because there are competing goals. If you increase use of commercial systems, particularly in electronics, your goal could be to reduce procurement costs. That can increase foreign content of military systems, either from imports or domestically produced components from foreign manufacturers.

This illustrates the larger dilemma of maintaining a national defense industrial base in a globalized high-technology sector. There must be greater recognition of tradeoffs between very low-cost, increased foreign dependence, and incurring the higher cost of a middle-ground alternative that might preserve certain dual-use domestic capabilities at the cost of, perhaps, longer insertion cycles or higher buy costs.

COOPER: So much of military systems today is electronic, and so much comes from the Far East, Europe, and elsewhere, that it's no longer possible for the DOD to claim it must have domestic suppliers for everything. Electronic products from the Far East can also be superior to even Defense Department equipment in their ability to operate in extreme environments. Clearly, they are much less costly. However, for certain things a domestic supply might be absolutely critical, as for a particular weapons system or something nuclear.

This country will always be allied with nations that can provide most of the critical things we cannot or choose not to provide. We can rely on them provided we make sure that, as the geopolitical continents shift, we take a clear look and find alternative suppliers in other parts of the world. It's clearly manageable. The benefits to the DOD from going the commercial route and buying off-the-shelf might be great enough to measure the savings in orders of magnitude—in decibels.

The Government is going to have to change the way it does its acquisitions. There's a lot of sentiment within the Defense Department to do this; yet it is very tough to get a bureaucracy to move on an issue as fundamental as the way it buys its equipment. This is a place where [professional/technical] and industry associations like the IEEE and the AIAA [American Institute of Aeronautics and Astronautics] and others can help get high-level defense and procurement officials to relax on the issue of requiring mil specs and the detailed specs of the parts and subsystems and so on in the weapons systems procurements.

Dealing with obsolescence

SCHELL: Another serious issue to the Defense Department is resupply. One of the aspects of commercial supply is that when ICs, for example, are no longer profitable, industry will no longer make them. What happens then?

MERRIFIELD: That's where flexible computer-integrated manufacturing facilities can come in. They have memories: some of those things were made three years ago and now the DOD wants three more. You can program the equipment and ship quickly because the memory is there with the quality and reproducibility needed. It obviates the need for keeping an inventory of more than you'll ever need, "just in case," and the cost of holding that inventory for 10 years and then disposing of it because it never was used.

COOPER: Another problem is that of the many, usually smaller, companies that handle build-to-print projects. Basically, they receive their designs and specs from the military departments and Government agencies. Then they just build the equipment the way it's presented in the request for proposal.

DOD is now specifying form, fit, and function compatibility for replacing parts and things that are out of production. These build-to-print outfits have to acquire a design capability. They have to hire higher-level design engineers that can take the form, fit, and function spec and, relying on computer-aided design (CAD) workstations, change it into designs using contemporary electronic parts.

You're going to see more of this. It will be an opportunity to redeploy the design capability now residing in the large aerospace companies. The engineers there might start moving to those smaller companies and serve not just the defense industry but others as well in form, fit, and function replacement of parts and systems.

SCHELL: The Government procurement side will have to do more than see to it that there is specification by part number. It will have to do better at functional specs by standardized architecture descriptions and storing data in a functional sense, rather than pinpointing the location of gates on a chip. That's going to require a new kind of enlightenment on the Government's part.

D. Bruce Merrifield: ***The key to consortia management is to set them up with a chief executive officer and a management staff, and the participating companies as limited partners. Then, by law, the partners should not be allowed to micromanage day-to-day operations.***



SCHELL: What are your views on the short-term effect on the defense industry of the current Mideast deployment?

COOPER: It will have a significant short-term effect, basically in three areas. First, it will delay somewhat the decline in the defense budget, and have a measurable effect on the '91 budget. More money—US $10 billion or so—will be pumped in for supplying equipment and paying for transport and things of that sort. There are 450 aircraft over there. All their equipment suppliers will get contracts for replenishing spare parts. There will also be cases of companies making a product that fits right into the military's requirements in the Gulf.

One small private company I know was supplying about 70 percent of the world market for global positioning-system (GPS) receivers. A year ago it developed a rugged version of the satellite receiver for

hikers and backpackers to take into the boondocks so they wouldn't get lost.

The U.S. Army ordered about 1000 for testing. When the Persian Gulf crisis arose, the Army, which had distributed those units all over the map, gathered them in, and sent them to Saudi Arabia. It immediately requested a contract for more. They'll be coming off a commercial production line.

Clearly, there was a benefit to the Defense Department in relying on a commercial producer for off-the-shelf equipment. It is getting its units fast and at a price at least 10 decibels cheaper than for militarized versions produced in small quantities by the aerospace industry.

The second effect of the Persian Gulf crisis is that it will yield a lot of experience in testing equipment in extreme conditions by the people who have to use it. Such testing had been just too expensive. It will likely help us form our opinions and plans and programs for supplying such equipment to the military over the next 10 or 15 years for such regional conflicts. This is probably the most likely type of conflict that the United States will find itself in.



David Mowery: ***The U.S. Federal government, almost alone among industrial countries, provides little assistance for restructuring for individual workers.***

The third effect is less tangible, but definitely on the plus side. It will give the industry some breathing room, some time to figure out on its own what it's going to do over the next five years. This could have incredible leverage for the future of the industry.

CURRIE: The lessons of Desert Shield are not new. They only reinforce a message that has been clear for some time: the world remains an unstable and dangerous place. Threats to peace can arise suddenly and from unexpected quarters. You have to be prepared, and with superior forces.

But "superior" need not be defined as greater numbers. Today the technologies embodied in defense electronics have become the linchpin to giving us that superiority.

Desert Shield demonstrates this. The desert heat may inhibit daytime operations, but U.S. forces own the night—for now. Iraqi forces may have five times more men and tanks on the ground—and the potential to put five times more planes in the air—but smart weapons offset those numerical advantages. At the same time, capabilities for surveillance and command and control provide yet another technological edge.

Upgrades and quantum leaps

The challenge for defense electronics is clear. It is to continue to equip U.S. forces with superior capabilities.

This requires a dual-track approach. The essence is balance: to pursue upgrades and quantum leaps at the same time. This means continuously applying technology improvements to extend the operating performance of existing systems, while simultaneously investing in the research and new technologies for the next leap forward.

Continuous upgrades ensure that our forces have the advantage when suddenly forced into the field. At the same time, investing in new technologies is the only prospect of fielding totally new and decisive capabilities in the future.

To pursue either course at the expense of the other is to invite disaster. A commitment to upgrades-only may keep our forces technologically superior for a while. But it virtually guarantees surprise and vulnerability when someone else's breakthrough renders our capabilities obsolete.

On the other hand, neglecting upgrades while pursuing leapfrog technologies and systems is equally hazardous. In today's budget environment, both DOD and industry must strike the right balance between the two options. President Bush's recent call for an "active and inventive program of defense R&D" gives us an opportunity to reach a much needed consensus on the right balance.

In national security, nothing is more certain than uncertainty. The extraordinary changes within the past year—or in the past few months—reinforce that point. A balanced dual-track approach to defense technology is a hedge against the uncertainties of the future.

Long-term implications

SCHELL: What do you see as the long-term implications of the crisis, particularly in the thrust of technologies where the DOD might shift its resources?

MERRIFIELD: The two elements that must be anticipated in similar crises are the use of chemical weapons and the possibility of nuclear capability by an Iraq or Libya or some other country. Preventing, or handling, these threats will take more than just the Awacs (airborne warning and control system) and good intelligence. There must be a capability to intervene physically and neutralize the threat. It should be such a deterrent that nobody would risk it, even a nut.

SCHELL: In the past, we've had only one class of weapons to deal with in such Third World situations, thanks to our Soviet and Soviet-oriented Cold War opponents. We now confront situations in which conceivably there are U.S., European, Soviet, and Third World weapons. This sets up a whole new array of challenges. From the standpoint of surveillance and intelligence, it is no longer just knowing what the Soviets have. It is knowing who sold what to whom and when, and where it is now. Stinger missiles are the most obvious.

COOPER: We're going to see heavier procurement of weapons by all the Middle East countries. They're going to want forces they hope would deter such an incursion as the Iraqis made into Kuwait.

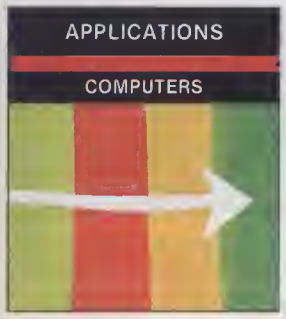
The question we'll have is ensuring that those weapons, if used against us, can be countered. The defense industry will be concerned with developing survivable platforms and signature detection systems and the ability to counteract sensors of all varieties. Clearly, there's going to be an emphasis on stealth technology in general.

We may also wind up with an expanded infrastructure from which military operations can take place in that part of the world. Near-term procurements will emphasize the equipment needed to transport aircraft and mobile forces, the airborne infantry, and the marine amphibious forces. That part of the industry will get some attention.

Increased attention will also be paid to intelligence gathering. The RPVs [remotely piloted vehicles] that the military disdained in the past are in great demand over there today. They're doing tactical Sigint [signal intelligence] and tactical Elint [electronic intelligence], and they're getting all kinds of information that makes it very easy to plan hour by hour how to counter the opposing forces. ◆

Designing with fuzzy logic

Insights into the application of a technology largely ignored in the West, but finding success in commercial and industrial problems in Japan



Japan has caught fuzzy logic fever. New products ranging from auto-focusing cameras to industrial assembly controllers are flooding the country. An air conditioner from Tokyo's Mitsubishi Heavy Industries Ltd. owes a power reduction of 20 percent to the use of fuzzy control algorithms alone. More than 70 percent of all washing machines currently manufactured by Matsushita Electric Industrial Co. in Osaka are fuzzy controlled, so great is consumer demand for the technology. Probably the best-known example is the subway system in Sendai, which stops with three times the accuracy of a manually controlled train and accelerates so smoothly that passengers find handrails superfluous.

The rest of the world, though, has yet to be bitten by the bug. Only a handful of organizations outside Japan are involved in the field, mostly with a research, not product, orientation. But companies everywhere are beginning to realize the value of this technology, as products with fuzzy logic control systems prove their versatility.

Fuzzy logic is a misnomer. Developed by Lotfi A. Zadeh of the University of California at Berkeley, it is firmly grounded in mathematical theory. Combining multivalued logic, probability theory, artificial intelligence (AI), and neural networks, it is a digital control methodology that simulates human thinking by incorporating the imprecision inherent in all physical systems. In traditional logic and computing, sets of elements are "crisp"; an element either is an element of a set, or it is not. For example, a temperature controller on a room heater might react to 35° C as "hot," but to 34.9° C as "cold." Such a sharp boundary would cause abrupt changes in a conventional control system's output.

In contrast, fuzzy logic works by turning the hard-edged world of binary control variables (hot/cold, fast/slow) into "soft" grades (warm/cool, moderately fast/somewhat slow) with varying degrees of membership. A temperature of 20° C, for instance, can be both "warm" and "a little bit cool" at the same time, a condition ignored by classical logic but a cornerstone of fuzzy theory. After all, precision is not always wanted: if the temperature in a house is 26° C instead of 25° C, the occupants couldn't care less. "Precision is expensive," acknowledged Ronald Yager, director of the Machine Intelligence Institute at Iona College, New Rochelle, N.Y. "Fuzzy logic is useful just because of its low specificity; it allows a more flexible response to a given input." The output of a fuzzy system is smooth and continuous, ideal for the control of continuously variable systems such as electric motors or positioning systems.

Fuzzy systems base their decisions on inputs in the form of linguistic variables [figure, p. 105]. The variables are tested with a small number of IF-THEN rules, which produce one or more responses depending on which rules were asserted. The response of each rule is weighted according to the confidence or degree of membership of its inputs, and the centroid of the responses is calculated to generate the appropriate output. Fuzzy logic shares the IF-THEN structure of AI, but unlike AI it is not a symbolic process, and employs few rules. Neural networks resemble fuzzy logic, but assign discrete weights to each stimulus, whereas fuzzy logic functions as a continuously valued state machine.

Kevin Self Correspondent

When to think fuzzy

In general, fuzzy logic is best applied to nonlinear, time-variant, ill-defined systems. If a system can be represented by a simple equation, it should probably be modeled with a straightforward control technique. In the case of a simple thermostat, upper and lower boundaries can be set to switch a heater or air conditioner on or off to stabilize its response about a desired temperature. Traditional proportional, integral, and derivative (PID) control systems will remain an accurate and cost-efficient solution to control problems involving simple, linear systems.

But if the system to be controlled is very complex, or cannot be easily represented by a series of IF-THEN rules, fuzzy logic may be the way to go. PID systems are designed to control a single output on the basis of a few independent inputs. Because of this independence, adding further inputs to the system rapidly complicates the control paths and requires the recalculation of all transfer functions. Adding another input to a fuzzy system, on the other hand, requires only the addition of another membership function and associated rules.

In system control, the fuzzy approach has a distinct edge over conventional methods. "Preprocessing" a large range of values into a small number of membership grades reduces the number of values that the controller has to contend with to make a decision. Because fewer values have to be evaluated, fewer rules are needed, and in many cases a fuzzy controller can solve for the same output faster.

Another strength of fuzzy logic is that it deals with observed, rather than measured, variables of the system. In system model-

Defining terms

Degree of membership: the "confidence" or "certainty"—expressed as a number from 0 to 1—that a particular value belongs in a fuzzy set.
Fuzzy logic: a branch of logic that uses degrees of membership in sets rather than a strict true/false membership.
Linguistic variable: common language terms used to describe a fuzzy set, such as "hot," "slow," "very cold," or "medium."
Membership function: a formula used to determine the fuzzy set to which a value belongs and the degree of membership in that set.
Neural networks: a study of intelligence that represents data and decision structures like a neural system. It assigns relative weights to data and is capable of supervised and unsupervised learning.

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ing, this means that users can indirectly evaluate more variables than with a conventional PID controller.

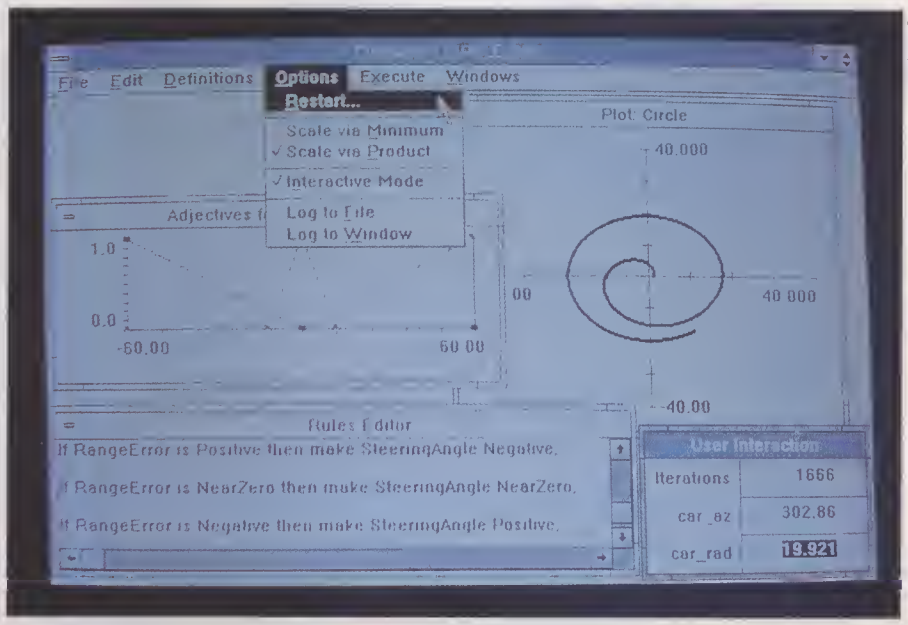
In traditional control modeling, the first step is to derive a mathematical model to describe the system. This requires a detailed understanding of all variables in the system—not always easy or possible if the system is very complicated. In contrast, fuzzy modeling deals with the relationship of the output to the imput, lumping many parameters together. This translates into the inclusion of higher-order variables, so that the resulting control system is of a higher order and often provides a more accurate and stable response.

The greater simplicity of implementing a control system with fuzzy logic can reduce design complexity to a point where previously insoluble problems can now be solved. Fuzzy systems typically result in a 10:1 rule reduction, requiring less software to implement the same decision-making capability. That was why engineers at Sanyo Fisher USA Corp., Chatsworth, Calif., turned to fuzzy logic for their video camcorder design when they discovered that, if they used conventional control methods, the microcomputer they favored would lack enough memory to implement all the functions they wanted. The fuzzy system reduced the amount of software needed to determine the optimum focus and lighting levels, allowing the functions to be implemented without external memory.

Rapid prototyping is another strength. Engineers at Rockwell International Corp.'s Science Center in Thousand Oaks, Calif., have applied fuzzy logic to the control of engine idling. Because the engine's variables (ignition timing, RPM, air flow) can be represented by a relatively compact set of equations, the application of fuzzy logic improved little on conventional control methods. The time that it took to implement the fuzzy logic controller, however, was an order of magnitude less than the time it took to develop the conventional system.

"The fuzzy approach is a good way to get started with little information," said Alan Firstenberg, the center's director of information sciences. The similarity between human thinking and fuzzy logic facilitates understanding and troubleshooting fuzzy control systems, a big plus when trying to bring a product to market in a timely fashion.

Still, fuzzy logic's strengths are also its drawbacks. Because it is a model-free estimator, it is difficult to develop a model that can prove the stability of such a system. Some designers feel uneasy using a theory that is fuzzy. "There is a definite need for stability analysis and validation tools for fuzzy logic," noted Rockwell's Firstenberg. Even so, fuzzy logic compares favorably with other intelligent control approaches, and PID control systems can be used in conjunction with fuzzy systems to ensure stability.



Ford Motor Co.

[1] CubiCalc, from Hyperlogic Corp., of Escondido, Calif., is used to develop and debug a fuzzy logic rule base to keep a car traveling in a circle at a constant radius. The software allows the user to vary parameters such as membership functions, and rule and fuzzy set adjectives.

Learning the rules

The first step in designing a fuzzy controller is to understand and define the system in terms of its input and output variables. Generally a control system measures a parameter and its rate of change as two of its inputs. Canon Inc. of Tokyo, in its H800 autofocusing camera, uses a charge-coupled device (CCD) array to measure the clarity of an image in six regions of the screen, thus determining if the image is in focus. Because the lens moves during focusing, the camera also measures the rate of change of focus, and slows the movement of the lens to avoid overshooting the optimum focus. The Canon controller uses 12 inputs: six to measure instantaneous clarity for each region of the screen, and six to measure the rate of change as the image comes into focus in each area. There is one output, the position of the focus lens.

Once the variables are known, they must be subdivided into membership functions. For example, if the input is temperature, then the linguistic values used might be cold, cool, moderate, warm, and hot. Typically, three, five, or seven values are used, ensuring a symmetrical distribution of positive and negative values around the median.

The key to success with fuzzy logic is to use just a few rules. If the membership functions have been constructed accurately, only a small number of rules are needed. Canon employs 13 rules in its auto-focusing camera, requiring only 1.1 kilobytes of memory to implement. The power of a small rule base has been demonstrated at the Ford Motor Co., Dearborn, Mich., where a fuzzy logic application using just three rules backs a simulated tractor-trailer into a parking space without jackknifing: IF the truck is near jackknifing, THEN reduce the steering angle; IF the truck is far away from the dock, THEN steer towards the dock; IF the truck is near the dock, THEN point the trailer directly at the dock. Researchers at Ford first studied the operation of a neural network controller based on a similar program developed by Bernard Widrow of Stanford University in California, and from it were able to infer the rules necessary to build a fuzzy rule base that performed the same function but took much less time to develop and radically simplified the learning process.

The method of studying the I/O relationship, defining the membership functions and the rules, depends on the type of system being modeled. In developing a model, the most straightforward approach is to study a human-controlled system. Because human beings think in terms of membership functions and use linguistic variables spontaneously, it is actually easier to start by interrogating people than with a mathematical model—a break with standard engineering practice. The same method can be applied to physical systems that, while automated, still follow human-type rules.

A good example of the direct application of human input to the design of a fuzzy system is the development of the electronic continuously variable transmission (ECVT). The ECVT-II, used in the Subaru Justy automobile, employs a fuzzy logic control

system to continuously adjust the position of a belt that changes the transmission pulley ratio and hence the car's acceleration and performance. Subaru (now part of Fuji Heavy Industries Ltd., Tokyo) questioned test drivers about their response to different pulley ratios to define what belt position on the pulleys corresponded to maximum performance without uncomfortable acceleration. The data from the drivers' evaluations was then used to generate the membership functions that governed the shifting.

Designing a fuzzy controller for a system with embedded rules, and hence ones that are not obvious, is more complicated. The most promising approach is Differential Competitive Learning (DCL), developed by Bart Kosko at the University of Southern California, Los Angeles, which uses neural networks to study a control system. Data to the existing controller is compiled into a series of I/O vectors and fed into a neural network. Predefined membership functions are assigned to the inputs and outputs, and the network is studied to find clusters of data indicating the presence of a rule. By adaptively quantizing the I/O vectors, this method can evolve a fuzzy logic rule base by interrogating an existing control system. Other researchers are currently working toward automating the process of developing fuzzy rules from neural networks, bringing the learning abilities of neural networks to fuzzy systems.

After the rules and membership functions have been defined, the last step is to test the system for the proper output. If it fails the test, the membership functions and/or rules should be adjusted. At this point, shapes of the membership functions are less important than their overlap, as the latter determines the characteristics of the transition between the two functions. Several iterations of this are done until the response of the system falls below a user-defined acceptable level of error.

A fuzzy controller

Although most work in fuzzy logic has been performed by in-house research teams at Japanese corporations, there are now two companies outside of Japan that specialize in fuzzy consulting. Togai Infralogic Inc., of Irvine, Calif., and Apt Instruments (N.A.) Inc., of Santa Clara, Calif., are both involved in the design of fuzzy software and systems for customers. Each has worked extensively with Japanese companies in developing fuzzy systems for customers.

Despite its differences from traditional PID control theory, fuzzy logic can be interfaced in many ways to existing control systems. "Don't rip out an existing system if it already works," cautioned Carl Perkins, cofounder of Togai Infralogic and independent consultant on fuzzy logic applications. "Use fuzzy logic to control the controller. [Just] add fuzzy reasoning to make up for the areas in which the conventional system doesn't do as well."

The simplest way to implement fuzzy logic is to reprogram an existing microcontroller-based system to reason fuzzily. Engineers at Togai Infralogic worked with Mitsubishi software on the development of the Beaver Warp air conditioner, rewriting the software for the 8-bit microcontroller already designed, requiring only minimal hardware modifications, but doubling the temperature stability of the system.

The small rule base and look-up tables needed for the fuzzy evaluations can be accommodated in the memory available with most microcontrollers. This allows designers to implement fuzzy reasoning with minor or no hardware modifications.

Membership functions for the inputs and outputs of the rules can be calculated ahead of time and stored in memory as look-up tables to speed up processing of the data. An alternative method involves numerically integrating the area of each output membership grade, but it is very mathematically intensive and may be beyond the capabilities of a simple microprocessor to calculate in real-time.

For more computationally intensive systems, a designer may wish to use a microprocessor with a custom reduced-instruction-set computer (RISC) architecture, storing membership functions and rules off chip. One such product, the FC110 Digital Fuzzy Processor from Togai Infralogic, handles up to 50 000 fuzzy logic inferences per second (Kflips). Basically a custom 8-bit, 10-million-instruction-per-second (MIPS) RISC, it has six macroinstructions specially designed to evaluate fuzzy inferences with up to 256 variables. The rule base is stored off chip in either RAM, ROM, or erasable programmable ROM.

Products utilizing fuzzy logic

Product	Company	Role of fuzzy logic
Elevator control	Fujitec/Toshiba	Evaluates passenger traffic to reduce waiting time and enhance car announcement accuracy
Golf diagnostic system	Maruman Golf	Selects best golf club for an individual's physique and swing
Video camcorder	Sanyo Fisher/Canon	Determines best focus and lighting when several objects are in picture
Washing machine	Matsushita	Senses quality and quantity of dirt, load size, and fabric type, and adjusts wash cycle
Vacuum cleaner	Matsushita	Senses floor condition and dust quantity and adjusts vacuum cleaner motor power
Hot water heater	Matsushita	Adjusts heating element to correspond to temperature and amount of water being used
Air conditioner	Mitsubishi	Determines optimum constant operating level to prevent power-consuming on-off cycling
Television	Sony	Adjusts screen brightness, color, and contrast
Handheld computer	Sony	Interprets handwritten input for data entry
Auto transmission	Subaru	Senses driving style and engine load to select best gear ratio
Stock trading program	Yamaichi Securities	Manages stock portfolios

Fuzzy tools

A number of tools are now available to help develop and model fuzzy control systems. CubiCalc, from Hyperlogic Corp. of Escondido, Calif., is a graphical development tool for fuzzy systems. A Microsoft Windows-based application, it allows the user to input rules in English sentences using qualifiers such as VERY, NOT, and SOMEWHAT. Membership functions are entered with a graphical editor so that their shape can be specified directly. The output of the fuzzy system can be displayed in tabular form or plotted.

The development of microcomputer code is necessary to implement fuzzy logic in a control system. Togai Infralogic has created the TILShell, a computer-aided software engineering (CASE) tool for building fuzzy expert systems with C language software. Users can define fuzzy sets, inputs, outputs, and fuzzy rules. TILShell compiles fuzzy logic rules directly into C language source code, which can be converted to code for any microprocessor with a C compiler. The software runs on either an IBM PC/AT compatible or Macintosh and sells for US $4600. Hardware accelerator boards using the FC110 fuzzy processor are available for IBM PC/AT compatibles and VMEbus systems, the latter capable of up to 1.6 Mflips when running four fuzzy processors. These boards allow fuzzy logic functions to be used as embedded controllers in larger systems.

(Continued on p. 105)

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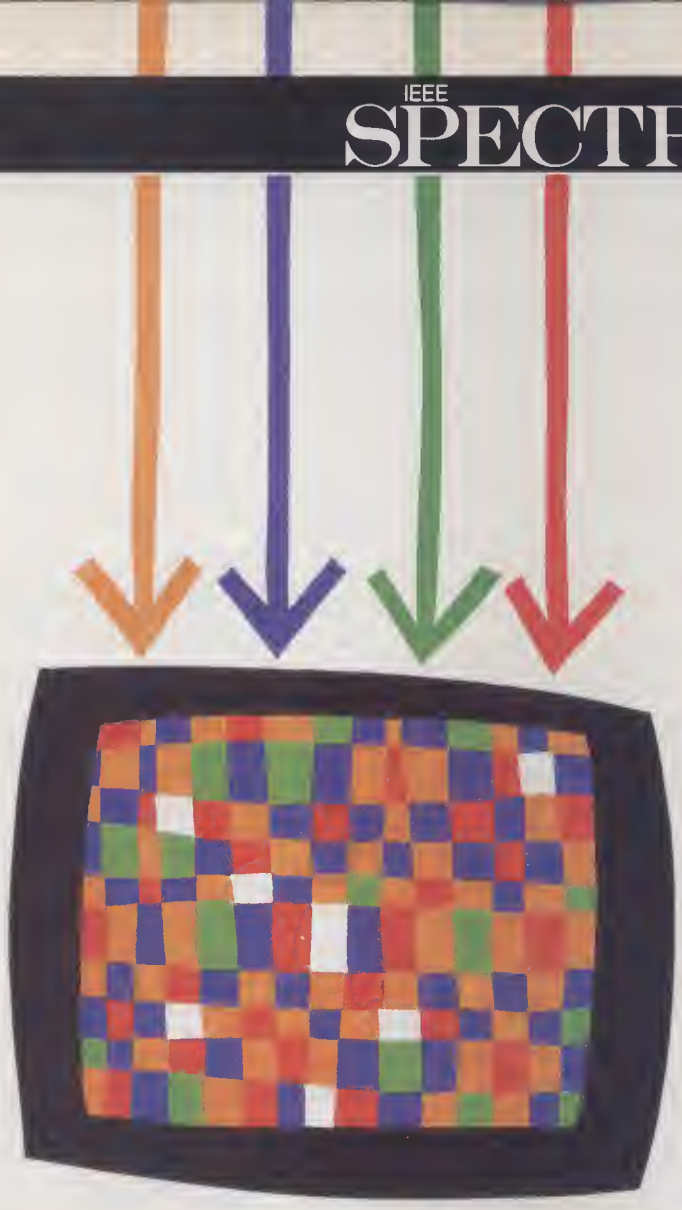
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SPECIAL GUIDE TO SOFTWARE

SYSTEMS, PACKAGES, AND APPLICATIONS

• DSP software • Affordable analog design • Electronic Design Interchange Format • Electromagnetic simulators • Computer-aided software engineering • Printed-circuit–board design tools • Data acquisition, analysis, and display • Frameworks • To probe further

As personal computers and workstations penetrate deeper into the electrical engineering environment, the importance of highly reliable and user-friendly software becomes clear. Without those characteristics, engineers cannot exploit these tools to the utmost.

In the last few years, many software packages for PCs and workstations have become available. They span the gamut from the electromagnetic design of electrical components to the creation of software systems. Even in today's highly digital world, analog circuits are still much in demand, as is software for designing them and simulating their operation [p. 60].

Furthermore, as the clock frequencies of microprocessors pick up, leads and conductors on a printed-circuit board come to behave like transmission lines, and here software packages for electromagnetic analysis by finite- or boundary-element methods come in handy. Not only do they typically replace tedious manual mathematical analysis with much simpler data entry, but they also enable designers to attack problems insoluble before. That these methods are gaining popularity is evident from the range of applications offered [p. 73].

As the variety and number of software design tools increased, engineers grew impatient with the complexities involved in exchanging information. As a remedy, a consortium of electronic design automation and semiconductor vendors devised the Electronic Design Interchange Format (EDIF) [p. 68]. Help is also coming from another industry effort—frameworks—which are specifications that describe how and what kind of data is to be presented to a computer-aided engineering software package. Leading design automation companies already supply software tools that conform to the industry frameworks [p. 90].

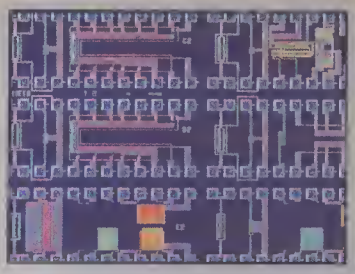
Software engineering, a discipline in its own right, has recently benefited from computer-aided software engineering (CASE) tools that not only help software engineers develop the programs but also allow more efficient maintenance and software management, among other functions [p. 78].

This guide provides, in tabular form, representative samples of available programs. Tables for digital signal processing and electromagnetic analysis were compiled by the authors of the articles on those topics; all others were done by *Spectrum* staff.

Gadi Kaplan Senior Technical Editor

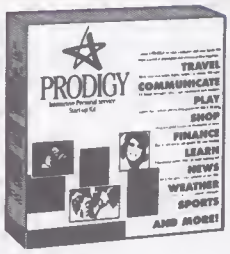
Defining terms

ALS: advanced low-power Schottky.
ASIC: application-specific integrated circuit; usually designed by the customer with automated tools provided by the manufacturer.
Assembler: a utility program that translates symbolic assembly language instructions into machine instructions or data on a one-to-one basis.
Axisymmetric: an object possessing an axis of rotational symmetry.
Behavioral model: a software model of a "black box" circuit whose output response to any input(s) is based only on user-defined equations; components inside the box need not be specified.
Block diagram: a drawing in which circuit functions are represented as blocks of various geometries.
Boundary-element method: a procedure for solving electromagnetic field problems by breaking the domains into smaller segments and by using integral equations in which the solution variables are confined within the boundaries.
CAE: computer-aided engineering, the use of general-purpose computers and special application software to automate routine, iterative hardware engineering tasks. (See also EDA.)
CASE: computer-aided software engineering, the use of general-purpose computers and special application software to speed and control software development.
CFI: Computer Framework Initiative, a consortium of computer-aided engineering (CAE) software users and vendors dedicated to creating a standard CAE framework.
CGA: color graphics adapter, a printed-circuit board installed in an IBM-compatible PC for color display.
Circuit simulation program: a computer program that mathematically predicts the behavior of circuits under various conditions.
Component diagram: a drawing in which circuit components, rather than functions, are represented. (See also Schematic.)
Connectivity: connections of a design, established by joining the pins of physical components or ports of logical components.
Consumer: In a framework environment, a software package that accepts data from a producer (which see).
DRC: design rules checker—software that examines a design to make sure it conforms to manufacturing rules.
DXF: Drawing Interchange Format—a standard format for transferring information to mechanical CAD programs.
EDA: electronic design automation, that branch of computer-aided engineering concerned primarily with design tasks. It is often used interchangeably with CAE.
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EGA: enhanced graphics adapter, an improved version of the CGA with higher resolution and greater color capability.
EICs: equivalent ICs (integrated circuits)—a way of expressing the component capacity of a layout package.
Embedded software: code not visible to the end user.
EMS memory: Expanded Memory System—implemented in software, a means of expanding the addressing capability of a PC DOS to more than IM byte. (See also LIM memory.)
FFT: fast Fourier transform.
Field-programmable gate array (FPGA): an array of gates on a chip whose interconnections can be arranged electronically by the user.
Finite-element method: a procedure for solving electromagnetic field problems by dividing the domain of interest into small, basic elements and by solving differential equations in each of those elements.
FIR filter: finite impulse response filter.
Force vectors: a tool to help achieve optimal component placement, force vectors are lines emanating from components, whose lengths and directions provide visual clues as to where components should be moved to minimize connection length.
GPIB: general-purpose interface bus, also called HPIB (Hewlett Packard Interface bus) and, more formally, IEEE Standard 488.2 interface. A byte-serial bus created to interconnect instruments and computers.
HPGL: Hewlett Packard graphics language, a widely accepted format for exchanging graphics data between computers and output devices, especially plotters.
IIR filter: infinite impulse response filter.
Integrated design environment: a program that allows data from one design tool to be used by others so that the designer can switch easily between tools. Environments may be proprietary or open.
JEDEC: Joint Electron Device Engineering Council.
JEDEC/IEEE library: standard libraries of components, logic symbols, and printed-circuit-board structures that can be called by a layout program.
Kurtosis: a mathematical function that determines the extent to which a frequency spectrum is centered around a mean or peak frequency.
LIM memory: a standard type of expanded memory system named for its originators: Lotus, Intel, and Microsoft. Sometimes called LIM EMS. (See also EMS, XMS.)
Linker: a utility program that ties different software modules into one entity.
Local approximation functions: functions used to approximate electromagnetic fields that are zero everywhere except over one, local element.
MCM: multichip module.
Mesh generation: the process of mathematically converting the geometric shapes encountered in electromagnetic field problems into many small pieces.
Migration path: a planned way of upgrading from lower to higher performance hardware or software with minimal changes.
Monte Carlo analysis: a mathematical technique that, by randomly changing component values, predicts the effect of statistical variations on circuit performance.
Netlist: an ASCII file describing the circuit elements and the way they are connected, as distinct from a pictorial representation in a schematic.
Parameter passing: the ability to assign a particular value to a circuit parameter in a generic model so that it can simulate a specific circuit. Without this ability, each model in a component library must be manually customized for a specific application.
Parts list: an ASCII file listing the kinds and quantities of components needed to fabricate the circuit. (See also Netlist and Wire list.)
PCX: a standard graphics format for IBM-compatible PCs.
PLD: programmable logic device—a device containing transistors that can be interconnected electronically by users to perform various logic functions. (See also FPGA.)
Point-and-click interface: a graphical interface that employs a pull-down or pull-over menu, or icons and a mouse. (See also WIMP interface.)
Postprocessor program: a computer utility that manipulates an output file created by a second, more important program—also called a back-end program.
Power keys: a computer interface in which certain simple key-stroke combinations perform the same function as opening a pull-down menu and selecting an entry.
Preconditioned conjugate gradient algorithm: an iterative technique for solving large sparse-matrix equations in which the solution is computed by minimizing the residual in successive orthogonal directions.
Preprocessor program: a computer utility that prepares an input file for efficient use by a second, more important program—also called a front-end program.
Producer: in a framework environment, a software package that generates information that can be used by another software tool.
Pull-down menus: a program interface that uses key words at the top of the screen to identify the starting location for menus that the user can make appear below them.
Pull-over menus: similar to a pull-down menu, except that key words appear at the left of the screen and new menus appear to the left of key words.
Quasi-TEM wave: a nearly transverse electromagnetic wave in which the electric and magnetic fields have small but nonzero components in the direction of propagation, so that the fields are almost but not quite transverse to the direction of wave propagation.
Real mode: a mode of operation that replicates that of an 8088-based PC to maintain compatibility for some programs. In real mode, an 80286- or 80386-based PC limits its addressing capability to 1M byte of RAM.
286-protected mode: a mode of operation that replicates that of an 80286-based PC, using 80286 instructions not present in the 8088. In 286-protected mode, the 80386 limits its addressing capability to 16M bytes of RAM.
386-protected mode: the normal mode of operation for 80386-based PCs, in which 80386 instructions not present in the 8088 or 80286 are used. The 80386 runs fastest in this mode and can address up to 4G bytes of RAM.
Rip-up and retry: a popular algorithm for trace placement that goes back and rips up previously laid down traces as necessary to optimize board layout.
Scalar field variable: a quantity that has a single, or scalar numerical value at every point in space.
Schematic: a diagram in which component parts, physical or logical, are represented by simple symbols and their connections are represented by lines.
SMT: Surface-mount technology.
Solid modeling: a technique used to create and represent three-dimensional shapes in computers.
Structured program: a program constructed of a basic set of control structures, each with one entry point and one exit.
Structured programming: a software development technique that incorporates top-down design and implementation, and strict use of structured-program constructs.
Subcircuit: a group of physically realizable components that performs a specific function, typically treated as a black box.
Translator: a computer system in which input information is converted to the same information in a different format.
WIMP interface: a program interface that uses windows (W), icons (I), a mouse (M), and pull-down menus (P). Windows and the Macintosh interface are both WIMP interfaces.
Window: in digital filter design, a type of weighting function. In graphical interface terminology, any area of a computer display temporarily dedicated to running a particular software-controlled task.
Wire list: an ASCII file describing how the components are physically interconnected. (See also Netlist and Parts list.)
XMS memory: Extended memory system—a technique for overcoming a PC's memory limitations using disk storage. (See also EMS.)





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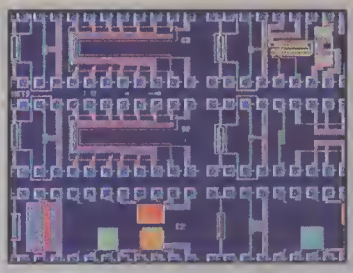
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CASE: computer-aided softw… the use of general-purpose cor… cial application software to sp… software development.
CFI: Computer Framework Ini… tium of computer-aided engine… ware users and vendors dedica… standard CAE framework.
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PCX: a standard graphics format for IBM-compatible PCs.
PLD: programmable logic device—a device containing transistors that can be interconnected electronically by users to perform various logic functions. (See also FPGA.)
Point-and-click interface: a graphical interface that employs a pull-down or pull-over menu, or icons and a mouse. (See also WIMP interface.)
Postprocessor program: a computer utility that manipulates an output file created by a second, more important program—also called a back-end program.
Power keys: a computer interface in which certain simple key-stroke combinations perform the same function as opening a pull-down menu and selecting an entry.
Preconditioned conjugate gradient algorithm: an iterative technique for solving large sparse-matrix equations in which the solution is computed by minimizing the residual in successive orthogonal directions.
Preprocessor program: a computer utility that prepares an input file for efficient use by a second, more important program—also called a front-end program.
Producer: in a framework environment, a software package that generates information that can be used by another software tool.
Pull-down menu: a computer interface that…
…simple symbols and their connections are represented by lines.
SMT: Surface-mount technology.
Solid modeling: a technique used to create and represent three-dimensional shapes in computers.
Structured program: a program constructed of a basic set of control structures, each with one entry point and one exit.
Structured programming: a software development technique that incorporates top-down design and implementation, and strict use of structured-program constructs.
Subcircuit: a group of physically realizable components that performs a specific function, typically treated as a black box.
Translator: a computer system in which input information is converted to the same information in a different format.
WIMP interface: a program interface that uses windows (W), icons (I), a mouse (M), and pull-down menus (P). Windows and the Macintosh interface are both WIMP interfaces.
Window: In digital filter design, a type of weighting function. In graphical interface terminology, any area of a computer display temporarily dedicated to running a particular software-controlled task.
Wire list: an ASCII file describing how the components are physically interconnected. (See also Netlist and Parts list.)
XMS memory: Extended memory system—a technique for overcoming a PC's memory limitations using disk storage. (See also EMS.)

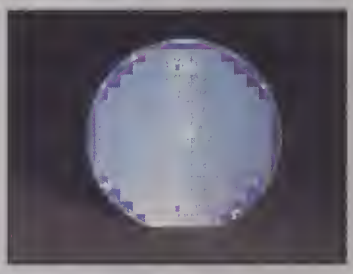
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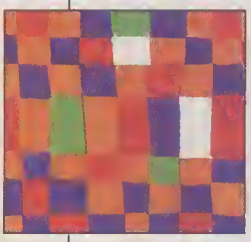
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Circle No. 201

Needed DSP software emerges

Hardware that can digitally handle analog signals ranging from the human voice to seismic echos is pushing the demand for software tools to simplify DSP programming



Digital signal processing (DSP) is on a roll. The technology is being used in numerous consumer and other commercial areas, in products ranging from talking toys to instrumentation for analyzing seismic returns in oil and gas exploration. The applications go on and on: compact-disc players, music synthesizers, biomedical monitors, studio-grade audio equipment, speech processors, programmable spectrum analyzers, and other intelligent laboratory instruments. And there are many military applications, too: broadband and frequency-hopping communication systems; conventional, synthetic, and array radars; lidar; sonar; and automatic target recognition. Although much of the popularity of DSP is due to the increased availability of low-cost DSP integrated circuits, an enlarged base of experience in the use and programming of these DSP engines has played a role. A growing number of hardware DSP accelerator boards, which are useful for prototyping new applications, has also contributed largely, as have the expanding collection of proven application development libraries and the appearance of more and more DSP development tools for the ubiquitous PC.

Those tools fall into two distinct categories, which correspond to the two main branches of digital signal processing: packages whose jobs are mainly signal acquisition and manipulation, and DSP programming environments. The former are of interest to laboratory data-acquisition engineers, to whom DSP simply means digitizing a signal and then manipulating it off-line for analysis, whether or not an actual DSP IC is used. The latter will appeal mainly to hardware engineers who are interested in programming ultrafast DSP chips for embedding in systems of various types.

Among the many software packages whose jobs are mainly signal acquisition and manipulation are such programs as ILS, DADiSP, LabWindows, DSPlay, and Asyst. These packages, which are often used to develop algorithms, come with assorted user interfaces: command mode, menu mode, icon-oriented, and some even based on signal-flow diagrams. They can turn a PC into a powerful data acquisition and processing workstation or instrument.

More general-purpose math packages, which manipulate vectors and matrices and can therefore perform signal processing, are also available. They might also be called "equation solvers" with a built-in "mathematical language," and they include Matlab, Mathcad, and Mathematica. These packages often include routines for performing such operations as fast Fourier transforms (FFTs), convolutions, signal arithmetic (adding and multiplying signals), simple filter design and application, signal generation (sinusoid, square wave, random), and statistical functions (mean, variance, extrema).

Even more important, they usually enable the user to manage signals, signal files, and data from analog I/O boards in a clear and intuitive manner. Those data management considerations become extremely important when large numbers of signals are collected for algorithm development. All of these software products make use of the advanced color graphics capabilities of the PC.

At the other extreme of the software spectrum are the DSP chip programming environments. Each DSP microprocessor has an assembler and linker associated with it that converts the DSP assembly language programs into executable DSP machine language. More sophisticated systems make available C compilers and a generous supply of library routines.

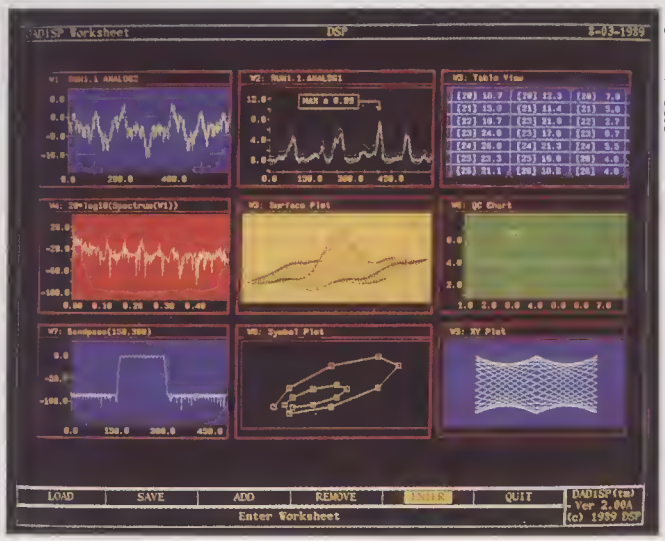
Library support is vital. There is no point in having every user write code to perform an FFT for every DSP chip he or she uses. That should be taken care of by library functions, just as is done for trigonometric functions. Of course, there are a wide variety of FFT algorithms available, which are optimized for various inputs and outputs, and a good library will offer an appropriately ample selection. For example, a simplified version should be offered for applications that need only the FFT magnitude rather than the complete complex FFT.

DSP debuggers are also available for DSP chips. Debugging programs may be for assembly language or for C. Debuggers permit the developer to stop the program at arbitrary points (breakpoints) and examine memory and registers. DSP simulators provide a means of testing the DSP machine code without having a expensive DSP coprocessor board in the PC. However, the DSP code is interpreted on the host processor, and so runs quite slowly.

Between the signal manipulation environments at one extreme and the programming environments at the other is a great deal of software designed to help the engineer write code for specific DSP products. Such programs as FDAS, Dispro, Hypersignal Plus, Monarch, DSPlay

(Continued on p. 54)

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Representative digital signal-processing packages for personal computers

Package	Company	Year first available	Price, US $	Min. memory, bytes	Algorithms and features	Code generator
BUG-56	Ariel Corp.	1988	$395	640K	Monitor and symbolic debugger	DSP56001
Monarch Professional, V 2.0	The Athena Group Inc.	1988 (V 2.0, 1990)	$595	640K RAM	5 FIRs, 8 IRs, state-variable, pole-zero and transfer function design, 7 IIR architectures, programmable signals/systems laboratory with 100+ DSP/math functions, extensive fixed-point support, FFT/IFFT, laser and plotter output, execute directly on selected board	TMS320C20, 25, DSP32, 32C, DSP56000/1, HSP43220
Digital Filter Design Package 3 (DFDP3)	Atlantic Signal Processors Inc.	1984 (V 3, 1990)	$1195 (add'l code generators $149)	640K	Price includes code generator for one DSP family; IIR, windowed FIR, Parks-McClellan FIR, graphical interface and analysis, automatic code generation	TMS320C10,15,17, 25, 30, DSP32
DSPlay XL	Burr-Brown Corp.	1988	$1495	640K	Graphical algorithm development for specific DSP chips; includes assembler	DSP32,32CC
DADiSP Version 2.0	DSP Development Corp.	1988 (V 2, 1989)	$1695	2M	Spreadsheet signal-processing system; FIR, IIR FFTs, power spectrum, convolution, signal generation	—
Tiger-30	DSP Research	—	—	—	C compiler and source debugger	TMS320C30
DSP Package	Galanco Spry	1988	$895–$1095 (includes hardware)	512K	FFT, signal and spectrum display, data acquisition software, waveform editor, assembler/debugger	Company's own TMS320C10- and TMS320C25-based PC plug-in boards
pF320/SSP	Forth Inc.	1987	$3050	24K	DSP development environment; extensive fixed-point math library; no filter design	Spectrum's TMS320C25-based PC plug-in board
Hypersignal Plus	Hyperception Inc.	1987	$489	384K	FIR/IIR filters user defined	ADSP 2100, 2101, DSP56000, TMS320C10,25, 30
InterTools Compiler/ Assembler	Intermetrics Inc.	1990	$2425	640K	Optimizations include instruction coalescing	DSP96002
MathCAD	MathSoft Inc.	1986	$495	640K	Mathematical equation solver; features include FFTs, multiple statistical functions. EE application packs available	N.A.
Matlab	The MathWorks Inc.	1985	$695–$1995	640K(PC) 2M (386)	IIR, FIR, spectral analysis 1-D and 2-D FFTs, correlation, convolution, decimation, interpolation, matrix computation with 2-D and 3-D graphics; signal processing toolbox option available	N.A.
NDP/FFT	Microway Inc.	1988	$250	2048K	Radix-2 FFTs for real and complex data; arbitrary-length FFT; 1-D and 2-D FFTs, convolution and correlation; autocorrelation; complex and inverse capstrum; Hanning, Manning, and Blackman-Harris windows; floating-point/integer and polar/rectangular complex-number conversions; supports arrays to 4G bytes	80386 or 80384 with appropriate Intel coprocessor (also includes Weitek support)
FDAS	Momentum Data Systems	1987	$495 (VI, basic)–$895 (V2, advanced)	640K	IIR/FIR, quantization effects, fixed-point simulation; compensation: D/A, comb, phase equalization	DSP32, ZP832, CAC DSP32-PC; LSI (Spectrum) DSP32; DSP56001, DSP96002; TMS32 on series Spirit-30
Lab Windows Advanced Analysis Library Version 2.0	National Instrument Corp.	1987 (V 2.0, 1990)	$895	2M	FIR, IIR, Butterworth, signal generation, FFT, FHT, convolution, correlation; triangle, Hanning, Hamming, Blackman and Kaiser Windows	N.A.
ILS family	Signal Technology Inc.	1978 (updated 1990)	$1000–$2000 with options	640K	Pattern recognition; FFT; IIR and FIR design, analysis, and development; power spectra, fixed/floating-point speech processing; convolution, quantization, compensation; data acquisition, file transfer/manipulation	Fixed point (through Momentum), floating point (through ASPI), SPOX server
Dispro V 2.0	Signix	1990	$395 (personal) $945 (prof'n'l)	384K	IIR, FIR, arbitrary-magnitude FIR, FFT, coefficient quantization and scaling, full simulation in fixed-point, time-domain plotting, signal generation	TMS320C1X,2X, ADSP210X, μPD77C25, DSP32C
Digital Signal Processing Library	Sonitech International Inc.	1987	$895 (source; object is $295)	640K	C library of DSP routines	Spirit-30
MacDSP	Spectral Innovations Inc.	1988	$2995	1M	DSP library for C, Pascal, Fortran, and Basic FFT, 2-D convolution, image filtering, data acquisition	Company's own DSP32C-based product

N.A. = Not applicable. — = Information not available.

(Continued on p. 57)

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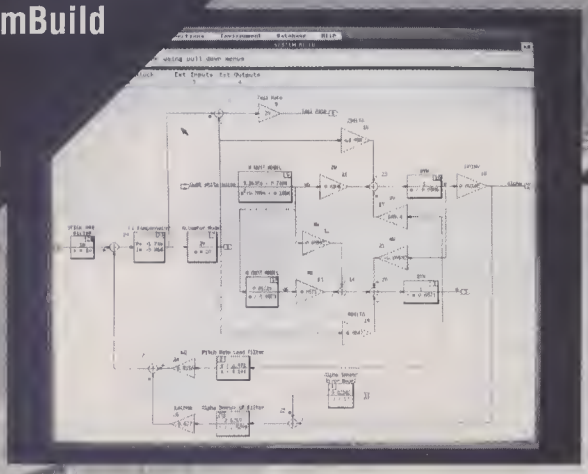
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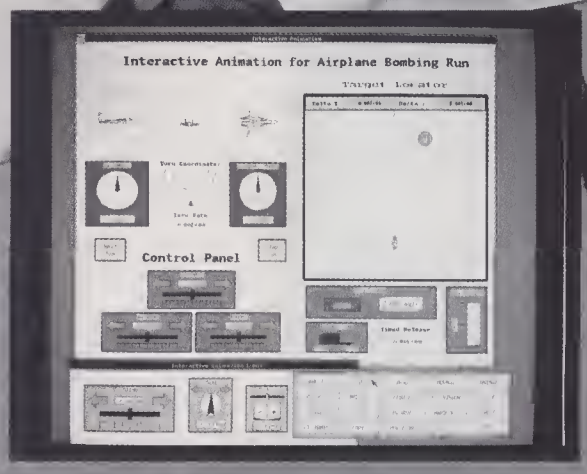
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Circle No. 205

(Continued from p. 54)
XL, and DFDP are available for the popular PC platform.

Of course, there is a limit to what can be done on a PC platform. PC-based software packages are best for modest projects with only one DSP engineer. For larger projects, which require several engineers, higher-end engineering workstation platforms, such as the Sun and MicroVAX families, are used, usually networked together for group-oriented signal-processing efforts. Software for such situations includes: Signal Processing Workstation and Block Oriented Network Simulator (Bones) by Comdisco, N! Power by Signal Technology Inc., ORYX Signal Processing Workstation, SIGX by Techni-Soft, and SonaGraph by Kay Elemetrics. Those packages do more (and also cost more) than the PC-oriented products considered in this article.

Digital filter design

A classic DSP engineering problem is filter design. A digital filter is most often used to remove unwanted frequency bands from a digitized signal, shape the spectrum, or modify the signal phase. It is the digital equivalent of a standard, active analog filter.

There are two main types of filters used in the world of DSP: finite-impulse-response (FIR) and infinite-impulse-response (IIR). FIR filters are always stable and have a linear phase response, which means that all frequency components of a complex signal undergo the same time delay in passing through the filter.

IIR filters require fewer stages to achieve the same performance as their FIR counterparts, but they can often prove unstable. Also, they cannot be designed to have linear phase, so they must be ruled out for many applications. Clearly, the choice of IIR or FIR depends upon the details of the application.

IIR filters

Although digital filtering techniques can realize functions not possible with analog circuitry, they are most often built simply by transferring analog designs to the digital domain. For example, the standard design methodology for an IIR digital filter is to convert the analog filter design in the s-plane to the digital domain by means of a bilinear transformation of the z-plane. In that transformation, the left half of the s-plane is mapped into the unit circle of the z-plane.

Classic filter types include Butterworth (maximally flat in passband), Chebyshev I (equiripple in passband), Chebyshev II (equiripple in stopband), elliptic (equiripple in both bands), and Bessel filter (group delay is maximally flat at dc). The s-plane to z-plane transformations are used because these analog filters are well understood and engineers are comfortable working with them—that is, design methodologies exist for creating analog filters to given specifications.

A good software package for DSP filter design today will let the user choose the type of IIR filter he or she needs. Most contain at least the first four filters mentioned above, although DSPlay omits the elliptic filter, which is widely used because it produces the lowest-order filter design.

Designing a filter requires the following information: sample frequency (which must be at least twice the maximum frequency component in the signal), pass-band and stop-band frequency specifications, pass-band ripple, and stop-band attenuation. From those values, the order of the filter can be estimated for each type of filter option. The Butterworth and Bessel filters will have the highest order and the elliptic will be lowest. The user picks the filter type and order, and the program goes on to compute the coefficients.

Estimation of filter order is a nice feature of obvious value, yet not every package has it. Some packages require that the user specify the order before the computer will compute the filter coefficients and frequency response. In such cases, if the specs are not met, the order may have to be increased. It is clearly preferable to know from the outset how big the filter must be before spending central-processing-unit time computing the coefficients and plotting the response.

Dispro by Signix, Wayland, Mass., has a small window that displays the estimated filter order for each of the available IIR filter types. When any of the design specifications are changed, the filter order is updated. That implementation has the added benefit of helping DSP novices get a feel for the tradeoffs involved in filter design.

FIR filters are classically designed with two different techniques: windows (not to be confused with a graphical window, X-windows, or Windows 3.01) and the Parks-McClellen (P-M) algorithm. Most filter design packages include both methods. When designing an FIR filter with a window, the user often must chose the type of window to be used. Most DSP software packages have a great diversity of windows to pick from: rectangular, Hamming, Hanning, Blackman, Kaiser, and so on. However, it should be pointed out that the Kaiser window is optimal and often the only window required. Optimality here means the user has control of the tradeoff between the width of a filter's transition band and the attenuation in its stop band.

The P-M algorithm generates the set of FIR coefficients that minimizes deviation from a given filter specification. Unless the filter requirements are too stringent (very narrow transition bands, for example), it will always converge to a solution. The P-M algorithm even permits arbitrary frequency specifications for performing any spectral shaping necessary. Both the P-M and window techniques are included in all the packages mentioned, though Monarch disguises P-M somewhat by calling it the Chebyshev FIR. Monarch, from the Athena Group Inc., Gainesville, Fla., also includes a "Max-Flat" FIR design module, which produces maximally flat pass and stop bands for low-pass filters. It is based on work by J.F. Kaiser.

As already noted, the DSP filter design process is filled with tradeoffs. The software package should minimize the effort the filter designer must put in to play with these tradeoffs. A well-designed package will not require the user to reenter filter specifications for every design iteration, but it will have a facility for easily modifying them after a filter computation cycle.

The ideal package will also produce frequency response plots with only one or two keystrokes (preferably automatically, when the design cycle is complete). Happily, most packages satisfy these simple criteria. An exception is DFDP (version 2.12), which requires renavigating the menu tree and reentering data for each design iteration. Monarch (version 1.7) requires going up and down a few menus and operations to get the frequency response plot of the filter. Version 2.0, however, corrects that shortcoming.

Most available DSP filter design software contains avenues for designing the previously mentioned IIR and FIR filters. The differences between packages are in the sequences in which information is entered and in the provisions made for evaluating tradeoffs.

Coefficient quantization

Once a filter has been designed and the coefficients stored away in a disk file, the engineer may consider the actual implementation. For off-line use (non-real-time), a floating-point high-level–language program can be written that uses these coefficients for the filtering operation. Some packages even implement the filter on a user-supplied signal with no further program development.

If a real-time system based on a DSP chip is being designed, it will be necessary to decide whether to employ fixed- or floating-point arithmetic. Until the past two or so years, DSP chips were strictly fixed-point devices. All the coefficients, internal filter values, and trigonometric functions were stored as fixed-point values, and all multiply and accumulate operations were done in fixed-point arithmetic. That led to certain critical difficulties in DSP filter implementation.

When floating-point filter coefficients are converted to fixed-point values in the process called quantization, subtle changes occur in the actual filter implementation. There will be slight changes in the pass-band and stop-band responses, and stable IIR filters may even turn into unstable de-

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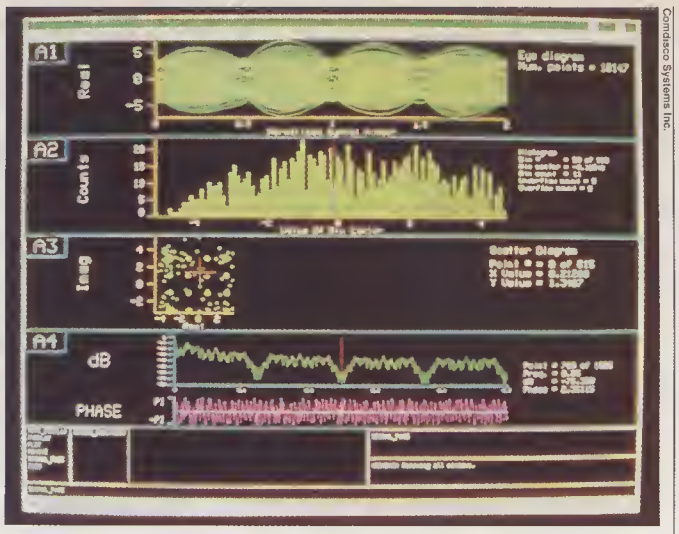
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Circle No. 225

For groups of engineers working on complex DSP projects, networked workstation tools are considered a necessity. Interactive analyses, performed by multitasking systems with linked charts such as those at right, let engineers quickly see the effect of changes while providing essential group communications.



Comdisco Systems Inc.

signs. A useful feature of DSP filter design software, therefore, is the ability to evaluate the response of the filter after coefficient quantization. The filter coefficients are converted into a fixed-point number of a user-specified bit-length (typically 15 bits plus a sign bit), and the magnitude and phase responses are plotted.

An IIR filter is usually implemented as a series of biquads (short for biquadratics—a ratio of two quadratic expressions in z–1). These biquads represent second-order stages in the filter, and configuration and ordering are important to minimize sensitivity to quantization and internal rounding and to eliminate internal overflow. There are many ways to factor the ratio of two large polynomials into a series of biquads; it is important to do it in one of the ways that will not cause trouble.

Another nice software feature is the automation of the biquad configuration, which minimizes sensitivity and eliminates overflow. Overflow is eliminated by computing the stage gain constant, which keeps the peak frequency response to 0 decibel (overall gain equals 1). John O'Donnell of Signix in his IIR filter designs has developed a "merged biquad" architecture that prevents internal overflow by controlling the gain at each stage of the filter. Only a couple of extra clock cycles are required to rescale the signal for each stage.

Real-time-filter implementation

Once the filter has been designed, the next logical step is to build a prototype to verify the design. Building a board from scratch would be a difficult, time-consuming endeavor, so DSP coprocessor boards exist for just that purpose. Such boards, which plug into a slot in the PC, are made by companies like Ariel, Atlantic Signal Processors, Burr-Brown, Dalanco Spry, DSP Research, Hyperception, Sonitech International, and Spectrum Signal Processing. In some cases, those companies sell boards that are actually manufactured by the DSP chip makers.

In many cases, the board vendors bundle third-party software with their products. For example, Sonitech, Spectrum Signal Processing, and Ariel all offer the Hyperception products for application and filter development. Burr-Brown Corp., which sells its own DSPlay XL, also sells Momentum's Filter Design & Analysis System (FDAS). FDAS filter designs can be imported in the DSPlay Flowgrams as filter modules.

Most DSP boards have one or two analog input channels, analog output channels, on-board analog-to-digital and digital-to-analog converters, and either a fixed-point or floating-point DSP chip. Some boards even have multiple DSP chips on board to increase system throughput. The large variety of boards match the large variety of DSP chips currently available. Additionally, several of the available filter design packages support a wide assortment of DSP boards and processors to the extent that DSP processor assembly language is produced, assembled, and linked into a complete program, ready to be downloaded and tested on the DSP board.

In the absence of a plug-in DSP board, it may be possible to check out the code with a piece of software called a DSP simulator. Such simulators are often available from the hardware board manufacturer or reseller. Simulators interpret the DSP machine code and actually simulate the DSP chip down to the register level. As can be imagined, the code-interpretation process is very slow and can therefore only verify the logical structure of the program. A simulator cannot ensure proper real-time operation.

Code generators

One stigma attached to DSP chips is that they are difficult to program. While some of the more recently announced DSP

chips operate in floating-point mode, the vast majority of available DSP engines on the market run in fixed-point mode.

Fixed-point mode virtually mandates that the chip be programmed in assembly language rather than in C or Fortran because a lot of attention has to be paid to scaling to prevent internal overflows during the calculation of intermediate results. It is not easy to have a C or Fortran compiler identify those points in the program where scaling will be an issue. Also, positioning the decimal point involves some delicate tradeoffs between dynamic range and precision, which are beyond the capabilities of any compiler in this marketplace.

Of course, assembly language is usually harder to work with than a high-level language. So one way for an application developer to quickly get up and going in a hardware DSP project is to have the assembly language code for a designed filter or module generated by the software package. Such code generators are becoming very common components of filter design packages. However, that still leaves the main program, I/O handlers, and flow control, which are usually required for a complete application, to be written the old-fashioned way—by hand.

Code generators often give the user some additional flexibility in creating the filter. That flexibility comes from specifying how memory is accessed and how looping is performed. For example, ASPI generates code for many different DSP chips from Texas Instruments, taking advantage of the unique instructions for each chip. If a TMS320C25 chip is used, the user can specify Direct Paged Memory, Indexed Memory, and Indexed Memory with Looping Control. He or she can also specify the additional internal precision if necessary—at the cost of extra clock cycles. Of course, each design choice entails tradeoffs that must be evaluated against the application and filter performance.

The term "code generator," by the way, is a bit of a misnomer. It refers to the software module that produces an assembly language program for a specific DSP chip or board-level system. Such a module takes generalized filter-design text files and fills in the holes in them with the coefficients and loop counters specific to the filter being designed. A separate text file might exist for each type of filter configuration, and the user selects the appropriate one.

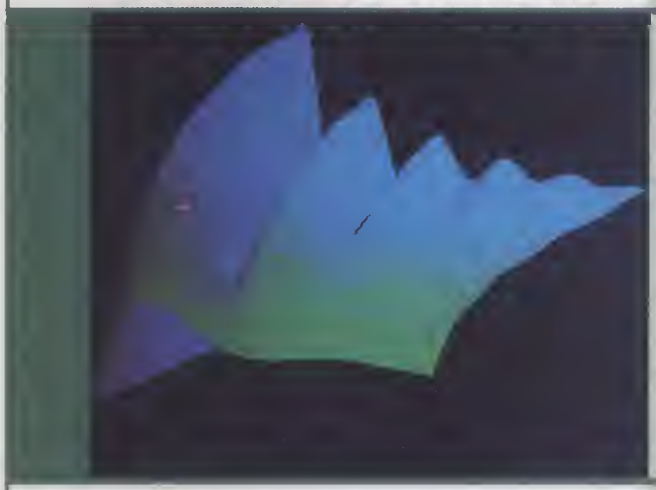
What to look for

Ideally, every DSP software package would have all the features now viewed as essential in such large-scale commercial software packages as word processors and spreadsheets—an installation program; a menu-driven interface; on-line help; support for many video, printing, and plotting devices; extensive documentation; and telephone support. Unfortunately, because

(Continued on p. 93)

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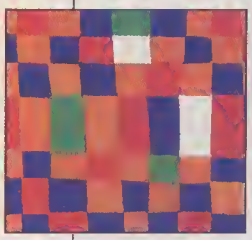
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Circle No. 217

Affordable analog design

Once the province of mainframes and minicomputers, software that significantly simplifies the design of analog circuits and systems can be found on PCs and MACs



Today's powerful personal computers are within the economic grasp of any engineering organization and can automate most of the jobs done by individual design engineers. And because PC-based analog circuit design systems involve minimum investment and organizational disruption, and hence are not a major corporate commitment, they are the ideal way for any company to begin finding out about the kinds of design tools available.

Ten years ago, a typical analog circuit designer did much of his or her work at a desk with pencil, paper, and handheld calculator, then verified the design in the laboratory. Today, he or she may still formulate a concept with pencil, paper, and calculator, but now will turn to a computer for all the other tasks. Math programs help develop equations to describe the circuit. Schematic capture programs help create block diagrams and subcircuits of transistors and other components. Component simulators help test and debug the subcircuits—and even the complete circuit. Graphics postprocessor programs simplify studying the results of the simulated testing and debugging. By using these tools, the designer can determine in advance and with a high degree of certainty whether the proposed circuit will work correctly when built.

Software that performs these functions can run on a variety of platforms: mainframes, workstations, and even personal computers. The accompanying tables, which list a wide variety of analog computer-aided engineering (CAE) software, give the platforms supported by a particular software package, along with other selection criteria.

The choice of the ultimate platform for integrating a company's engineering activities is not a simple matter. Some organizations need many engineers to work on a project simultaneously and to share a lot of information rapidly. A design may be extremely complex, requiring extensive simulation and closely coupled analog and digital circuit-level, system-level, mechanical, and software design. In these environments, a network of workstations linked to high-powered mainframes may be the only rational option.

John R. Hines Honeywell Corp.

But for many companies, PCs are the way to go. So it is worth exploring the analog design software readily available for these machines.

Writing and solving equations

Once a design concept has been developed, all analog circuit designers develop and solve equations that describe the proposed behavior of the circuit. The many different math tools that allow the circuit designer to do this on a PC can be grouped into two categories, depending on how they manipulate equations: symbolically or numerically.

Derive by Software House, Honolulu, Hawaii, and Chico Solver by Chico Software, Chico, Calif., represent two approaches to the problem of solving equations symbolically. Derive, at US $200 a relatively inexpensive program for IBM-compatible PCs, simplifies and solves most kinds of equations working engineers encounter. But as it does not use the Lotus-like pull-down menus of a WIMP interface [see glossary, p. 48], casual users will have problems using it. Chico Solver is a newer, more expensive (US $500) program for IBM-compatible PCs aimed more at scientists than engineers—it solves more kinds of equations than Derive. A designer can add math functions to Solver, an impossibility with Derive. Solver has unusual pull-down menus so it is still a difficult program for occasional users. Because their interfaces are arcane, neither program would be able to compete in the Macintosh market.

For numerically solving equations, MathCAD by Mathsoft Inc., Cambridge, Mass., and Matlab by The Math Works Inc., South Natick, Mass., are two tools available on IBM-compatible PCs, Macintoshes, and Sun workstations. (Matlab is also available on Apollo workstations, the Convex superminicomputer, and the Cray supercomputer for exceptionally involved problems, but few users will want so much power. Such problems in any case are usually easier to solve with a programming language than with a math tool.)

Both programs can numerically solve simple linear or quadratic equations, families of linear and quadratic equations or matrices, and equations or groups of equations with derivatives or integrals. They can also fit data to curves and plot two- or three-variable equations. Neither has a well-developed WIMP interface, even on the Macintosh, so they are difficult for the occasional user. Having sold more copies than all other math programs, the US $500 MathCAD is a popular standard against which all other math tools can be judged.

In its favor, MathCAD has almost 100 built-in functions, so it can solve almost any problem that can be stated in a few sentences or a paragraph. Its built-in func-

(Continued on p. 62)

1. Representative schematic capture packages for analog design

Package	Company	Year first available	Price, US $	Platforms	Library size
SpiceNet	Intusoft	—	$295	PC, Mac	100
Design Architect	Mentor Graphics Corp.	1990	N.A.	HP/Apollo	Variety of digital, analog libraries
Schema III	Omation Inc.	1985	$495	PC	7000 discrete parts; optional documentation symbol library (1000)
OrCAD/SDT III	OrCAD	1990	$495	PC AT/386, PS/2	6200 parts
ValidGED	Valid Logic Systems	1982 (rev. 1990)	$8800	Sun 3, 4; DEC 2100, 3100, 5400	Over 4000 components, including power components, transformers, and system-level functional blocks
McCAD Schematics	Vamp Inc.	1986	$495	MacPlus	N.A.

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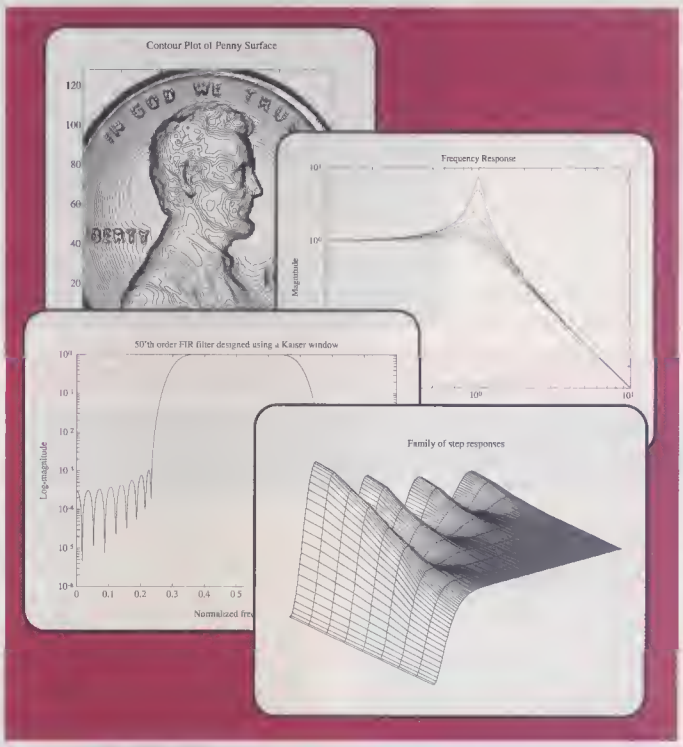
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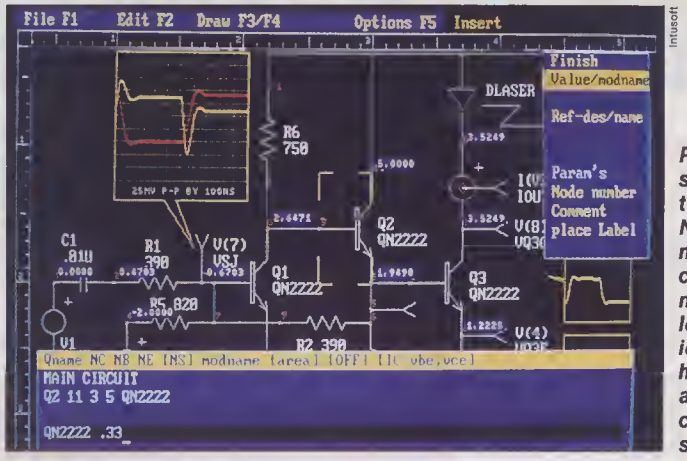
SP 11/90

Circle No. 216

(Continued from p. 60)

tions include the Bessel functions and the erf error function, which are solutions for common differential equations. MathCAD files are also self-documenting, so an engineer can keep track of solutions by keeping hardcopy of previous MathCAD files. It is reasonably easy to learn, despite an unusual interface that has neither pull-down menus nor a WIMP interface. An 800 help number offers free technical support.

However, solving problems with MathCAD is not always easy. It is not fast when solving simple problems that can be described in a sentence, and it gets much slower when solving problems that must be expressed in paragraphs rather than sentences. Also, the user may find it difficult to implement solutions that require complex logic or nested loops. The PC version of MathCAD can import graphics from only a very few programs.



Pull-down menus, such as the one on the right of SpiceNet screen at left, make the job of creating and manipulating an analog schematic easier. The waveforms have been back-annotated from a compatible Spice simulator.

2. Representative simulation packages for analog design

Package	Company	Year first available	Price, US $	Platforms	Multi-level	Internal mixed mode	Library size
Saber	Analogy Inc.	1985	$15 000	Sun, HP/Apollo, DEC	•	•	1200 analog parts, 3000 mixed-mode parts
ContecSpice	Contec Micro-Electronics USA Inc.	—	$1500–$9900	PC, Sun	•	•	2500 parts
MacSpice Professional	Deutsch Research	1987	$1195	Mac II, SE 30	•	•	2000+ parts
mWSpice	EEsof	1986	$8400–$15 400	PC (DOS and OS/2), Sun, HP/Apollo, DEC			576 s-parameter device data files, 93 FET device models, 9 BJT device models and more
Precise	Electrical Engineering Software Inc.	1990	$9500–$25 000	Sun, HP/Apollo, DEC	•		1000 analog parts
IsSpice	Intusoft	1988	$386	PC	—	—	—
AccuSim	Mentor Graphics Corp.	1989	$24 900	HP/Apollo	•		Over 3400 analog component models
HSpice	Meta-Software Inc.	1990	$3000–$90 000	PC, Sun, Apollo, DEC	•	•	Over 800 discrete-device models
PSpice	MicroSim Corp.	1984	$950-$4500 depending on platform	PC DOS and OS/2; Mac II, SE; Sun 3, 4, Sparcstation; DEC station 2100, 3100, 5400; HP/Apollo and others		•	3000 analog, 1200 digital
Schema Susie	Omation Inc.	1989	$995+	IBM PC/AT/XT/286/386/486		•	Optional libraries, microprocessors, PLAs, GaAs, RAM, ROM, EPROM (2000+ parts), CMOS/TTL standard—timing to picoseconds
SpicePlus	Valid Logic Systems	1984	$2000	Sun 3, 4; HP/Apollo; DEC 2100, 3100, 5400	•		4000 components, including power devices, transformer cores, nonlinear magnetics, as well as system-level function blocks
Classic Spice	Vamp Inc.	1988	$745	Mac II, SE/30	•	•	—

At twice the price (US $1000), Matlab has three times as many functions as MathCAD, so it can solve almost any problem, no matter how long or complicated. If it cannot, a user may create and integrate custom C code into Matlab to extend its functionality. If more memory is needed, versions of Matlab specific to machines based on 286 and 386 microprocessors are available that use all the memory an AT-compatible or 386-based PC can provide.

Matlab's interface is much like that of an integrated programming environment, so it has less structure than MathCAD and takes longer to learn and use; there are many detailed examples in the documentation, though. Further, a designer can extend Matlab to cover problems encountered in his or her area of expertise; by studying Matlab's several Matlab toolboxes, which contain extensions that solve common problems, a designer can learn how to write tool-extending code.

Drawing blocks and circuits

As the designer arrives at the equations to implement analog functions, he or she can begin to segment the design into functional blocks. For instance, having worked out the appropriate Bessel functions, the designer can use them to implement a filter function in the design. Then, the process of designing the filter with actual components can begin. To help in this process, the designer now has schematic capture programs.

Ideally, the schematic capture program meets three requirements [Table 1]. First, it documents the design by function (block diagrams) and by component (circuit diagrams). Second, it provides lists of the components needed for the design (parts list), the functional interconnection of components (netlist), and how individual component pins are actually wired togeth-

(Continued on p. 64)

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3. Representative postprocessor packages

Package	Company	Year first available	Price, US $	Platforms	Features
SpiceWindows	Deutsch Research	1987	$995	PC AT/286/386/486, PS/2	Runs under Windows 3.0; takes output from TurboSpice, PSpice, others; can paste into Microsoft Word; outputs to any printer supported by Windows
MicMask	EEsof	1986	—	PC (OS/2), Sun, HP/Apollo	HPGL, Gerber, GDSII, Wild Heerburg, Aristo
IntuScope	Intusoft	—	$325	PC, Mac	Pull-down menus, multiple windows, waveform calculator, multiple graph formats, digitizes waveforms for Spice input
Schema III	Omation Inc.	1985	$495	PC AT/XT/286/386/486	Netlist formats to all popular board layout systems; EDIF 2.0, ADF, DXF block output (parts transferred as whole, electrical parts—not a graphic representation); TIFF, PostScript; Schema board layout supports CAM postprocessors, DXF, and others
Statistical Analysis	Valid Logic Systems	1987	$10 200	Sun 3, 4; HP/Apollo; HP; DEC	Performs Monte Carlo analysis and sensitivity/worst-case analysis; analysis sensitivity

4. Representative integrated analog design environments

Package	Company	Year first available	Price, US $	Platforms	Tools
Analog Artist Design System	Cadence Design Systems Inc.	1989	$30 000	Sun 3, 4; HP/Apollo DN3xxx, 4xxx; DEC 3100, 5xxx	Schematic capture (parameterized and hierarchical), interactive simulation environment, Spice circuit simulator, graphics postsimulation analysis, waveform calculator; options: statistical optimization package, analog layout, analog place and route; physical design verification tools
CLIO	Electrical Engineering Software Inc.	1990	$18 750 (4 seats)	Sun, HP/Apollo	Schematic capture, simulation (Precise), yield analysis, design centering, optimization, graphics postprocessor
Academy	EEsof	1988	$6000–$19 000	PC (OS/2), Sun, HP/Apollo	Schematic capture, simulation control (linear and nonlinear circuit and system design), layout editor, integrated design documentation, postprocessor
Analog Station	Mentor Graphics Corp.	1989	$44 900	HP/Apollo	Schematic capture (Design Architect), simulation (Accusim), Monte Carlo analysis; option: analog library (Accuparts)
Schema Designer	Omation Inc.	1985	$1895	IBM PC/XT/AT/286/386/486	Schematic capture; board layout with manual, autoroute, or combination; four-algorithm heuristic router; Gerber photoplot; options: push-and-shove router (for complex boards, SMT both sides, multilayer), DXF, G*man
MicroCap III	Spectrum Software	1990	$1500	PC	Symbol (shape) editor; library editor; parameter estimation; ac, dc, and transient analysis; Monte Carlo analysis
Analog Workbench II	Valid Logic Systems	1990	$16 000	Sun 3, 4; HP; HP/Apollo; DEC 2100, 3100, 5400	Schematic editor; simulator (Spice Plus); integrated analysis tools for ac, dc, and transient analysis
McCAD EDS-2	Vamp Inc.	1988	$1895	Mac Plus (2M)	—

— = Information not available.

(Continued from p. 62)

er (wire list). Finally, the schematic should provide a means of creating the input to an analog simulator (Spice and its derivatives being the most popular analog simulators), so that the designer can test and troubleshoot the design before building any hardware.

There are several programs for schematic capture on IBM-compatible and Macintosh personal computers. McCAD Schematics, from Vamp Inc., Los Angeles, is a Macintosh implementation, while OrCAD/SDT III, from OrCAD, Hillsboro, Ore.; Schema III from Omation Inc., Richardson, Texas; and SpiceNet from Intusoft, San Pedro, Calif., are programs for IBM-compatible PCs. They are all roughly comparable to schematic drawing tools available on workstations and are priced in the US $400–$600 range. However, not all of them are suitable for analog simulation use.

The full-featured McCAD Schematics is part of the supplier's integrated environment for analog and digital circuit design and layout. The documentation that comes with McCAD Schematics is confusing and the details for most functions are omitted. Fortunately, the program has a fully implemented Macintosh interface, so it is easy to use. It has all the symbols needed to create analog circuit schematics and it creates partial Spice input files, too.

OrCAD/SDT III, the third major iteration of OrCAD's schematic capture program for IBM-compatible PCs, is a full-featured package. It uses a Lotus-like left-to-right pull-down menu interface and has power keys to complement the menus. On an 8-megahertz XT, OrCAD's pan, zoom, and redraw functions work about as fast as those of SpiceNet or Schema on a 6-MHz AT. Packed with utility programs, it is the drawing program of choice for digital circuit designers.

Unfortunately, if the schematic includes subcircuits, SDT III cannot be used to create even partial Spice input files: its Spice netlists cannot include components beginning with the letter X (which designates a subcircuit). In addition, SDT III does not always supply schematic drawing tools in a format usable for analog circuit designers: it took OrCAD a year to rotate the pnp transistor symbol so the emitter pointed up instead of down, and the library for PSpice (the most widely used analog simulator, from MicroSim Corp., Irvine, Calif.) still has minor bugs. A designer with some experience at software hacking can tinker with it and make it usable for analog circuit schematics, but it is not a turnkey solution.

Schema III is the fourth major revision of Omation's full-featured schematic capture program for IBM-compatible PCs. This revision added automatic component rotation (a feature SpiceNet and OrCAD/

(Continued on p. 66)

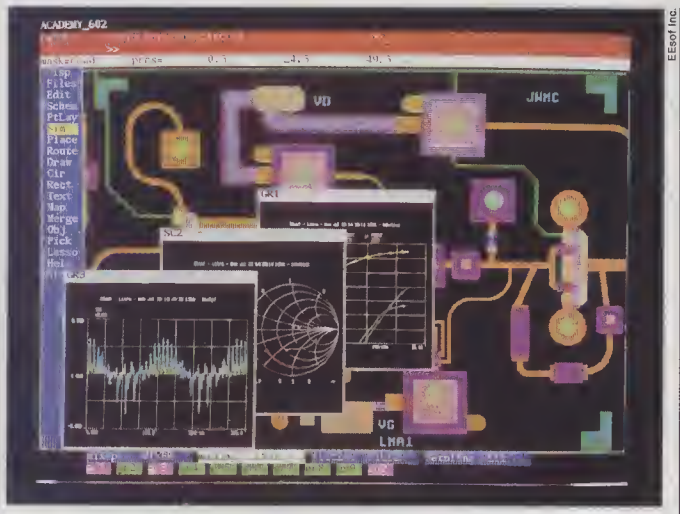


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In an integrated analog design environment, engineers can get an overall view of a circuit's performance quickly and try out changes more easily. In the Academy display at left, resimulation updates spectra and Smith charts.

(Continued from p. 64)

SDT have had for several years), on-line help, pop-up menus, and a powerful file manager. Its graphical performance is roughly comparable to SpiceNet's, a little slower than OrCAD's. It has a pull-over menu interface and power keys. Designers used to Lotus or other programs with pull-down menus will find the pull-over menus inconvenient. Also, complete Spice input files cannot be created from Schema.

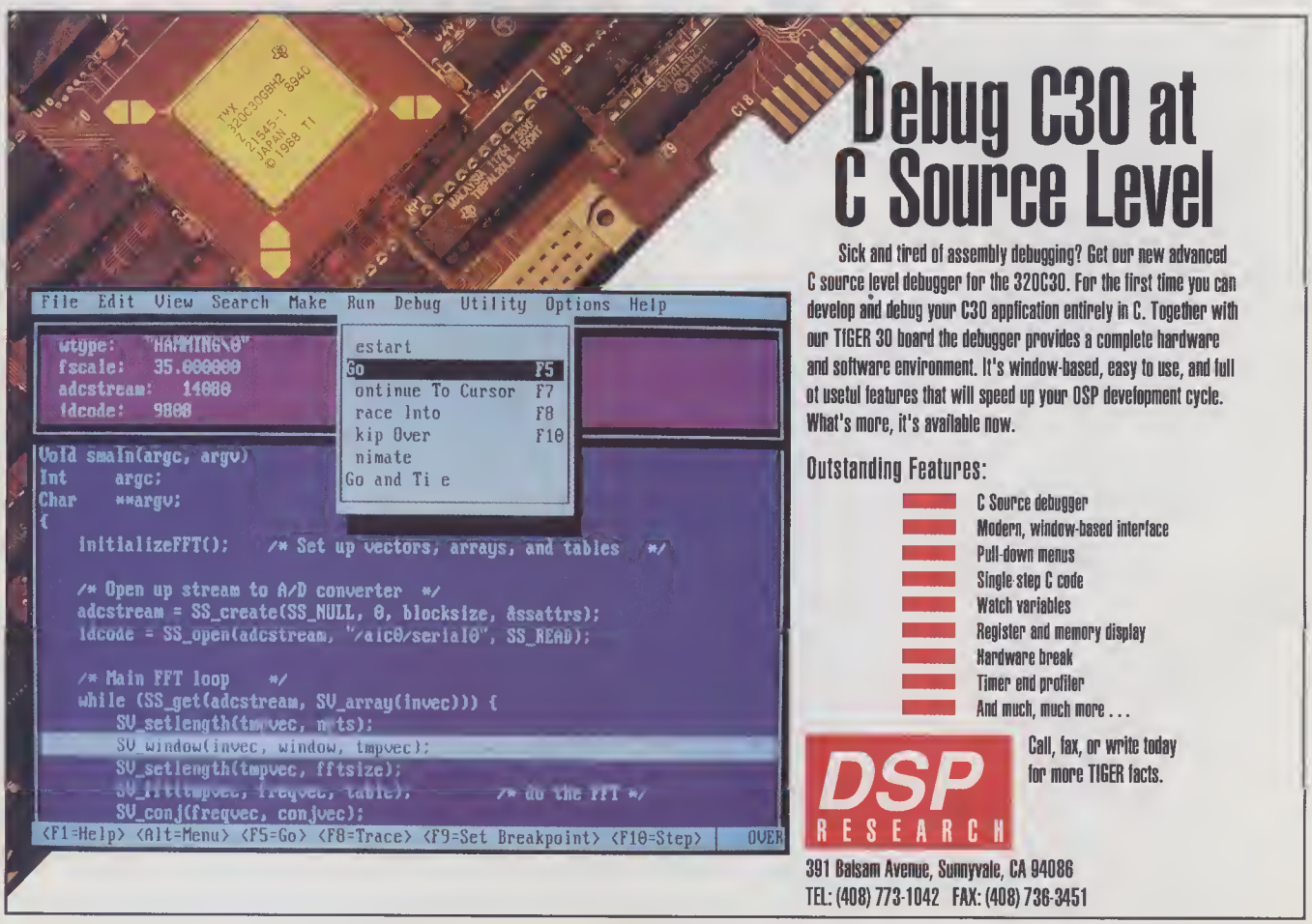
All the components in Schema are correctly configured for creating analog schematic drawings. It is a usable schematic capture program for both analog and digital simulation programs, particularly for designers who need to create large, complicated circuits. The tech support people at Schema understand analog circuits.

SpiceNet is actually a front-end program for Spice and is part of Intusoft's integrated-circuit design environment. Like Schema, it has a Lotus-like pull-down menu interface and power keys. For a single-page schematic, the jobs of component placement, redraw, zoom, and pan take less than a second on an AT-compatible PC. Its library contains several hundred components, including unusual ones like discrete power devices, vacuum tubes, and multiple-winding transformers. Moreover, when existing components are inadequate, it takes only a few minutes to create a new component. Complete Spice input files may be created and edited within SpiceNet, too.

This program is not a full-blown schematic capture program, however: it cannot create a parts list, wire list, or bill of materials, and its library does not support PSpice's enhanced component models. While it does handle the small, relatively simple circuits typically created by analog circuit designers without problems, it is sometimes less graceful at handling multiple-page drawings or large, complicated circuits.

SpiceNet works better, however, when used with PreSpice, Intusoft's Spice preprocessor. PreSpice contains a text editor for modifying Spice input files as well as code that converts functional blocks into subcircuits, passes parameters into subcircuits, and creates multiple input files for Monte Carlo analysis with Berkeley Spice. SpiceNet and PreSpice are compatible with PSpice and almost all implementations of Berkeley Spice.

The most important advantage that computer-aided analog design can offer engineers is the ability to check out circuit



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performance before making any hardware commitments. Analog simulators [Table 2] make it easy for the designer to try several alternatives and correct design oversights or flaws without major expense.

Simulation surveyed

The grandparent of most simulators on the market today is the Simulation Program with Integrated Circuit Emphasis, or Spice, developed at the University of California–Berkeley, in the early 1970s. Non-Spice based simulators—most notably Saber from Analogy Inc., Beaverton, Ore.—have also gained acceptance for high-level functional simulation; Saber can be found in most workstation environments, but its memory requirements have kept it out of the PC and Macintosh world. On the other hand, many versions of Spice are available for personal computers. These programs fall into two categories: proprietary versions derived from Berkeley Spice source code, like PSpice from MicroSim Corp., Irvine, Calif., and direct translations of Spice, like Classic Spice from Vamp and IsSpice from Intusoft.

PSpice began to diverge from the Berkeley Spice Fortran source code soon after the first version for IBM-compatible PCs was available. First, minor changes were made to the code so that it could be partitioned into two segments that were small enough to run comfortably on an IBM-compatible computer. Then, changes were made to the source code to improve convergence, to allow changes to the source code so users could modify the characteristics of Spice circuit elements or even create new elements, and to add a new Spice command that created an output file readable by a graphics postprocessor.

Making these changes was so difficult that MicroSim decided to convert its Fortran source code into C source code, which is more easily maintained, modified, and transported to other platforms. Easy modifiability has given MicroSim a big edge in the PC marketplace: only PSpice allows mixed analog and digital simulation, Monte Carlo analysis, and behavioral models.

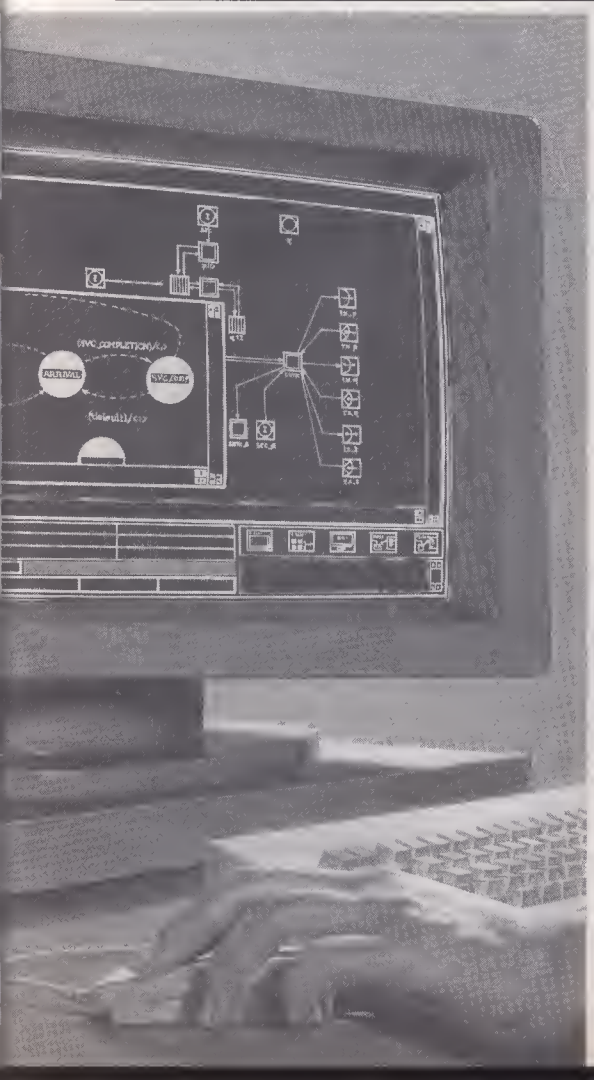
MicroSim offers three versions of PSpice for IBM-compatible computers: 8088 real mode (or DOS), 286-protected mode, and OS/2. The DOS version, slightly faster than either the 286-protected–mode or the OS/2 version of Spice, is limited to simulating circuits with fewer than 200 transistors. The 286-protected–mode program and the OS/2 version of the program can simulate larger circuits. The maximum circuit size for these versions can be estimated by the rule of thumb "250 transistors per megabyte of RAM," first proposed by Wolfram Blume of MicroSim. This results in a maximum of 4000 transistors for the 286-protected–mode version of PSpice, which does not allow multitasking, and for the OS/2 version, which does.

An experienced PSpice user may have mixed feelings about recommending MicroSim software to new users. MicroSim software typically costs two to three times more than equivalent products from other vendors. MicroSim software for personal computers still requires a copy-protection dongle and, if the dongle doesn't work, MicroSim does not have a fix. It now takes a long time for MicroSim to eliminate bugs: four years ago, a bug fix took one month; today, it takes a year to get the fix. Yet there's no getting around the fact that PSpice is a *de facto* standard.

Classic Spice, a very Mac-like implementation of Berkeley Spice 2G6 for the Macintosh, is part of Vamp's package of IC design tools for that PC. Its documentation is not detailed, but its fully implemented Macintosh interface makes it very usable. It also takes advantage of the Mac's multitasking operating system to open windows to schematics created by McCAD Schematics. However, most circuit designers will purchase a graphics postprocessor to complement it.

IsSpice is a full implementation of 2G6 Spice for the PC and Macintosh. Only minor changes were in the Berkeley source code for the PC version. The standard PC version of IsSpice will simulate circuits

(Continued on p. 93)

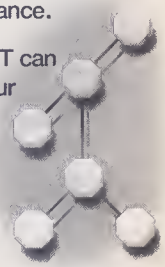


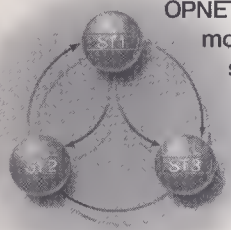
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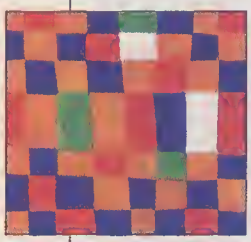
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EDIF grows up

It is now in its second full revision—a mature Electronic Design Interchange Format (EDIF) that is paving the way for universal data exchange among CAE tools



Computer-aided design uses a variety of tools that cannot communicate with each other directly. For example, a software package that designs a circuit schematic can seldom "talk" to the simulator package that checks the circuit's operation, which in turn cannot talk to the package that designs a printed-circuit board to embody the schematic, which cannot talk to the factory software packages that create artwork, drilling information, machine-insertion data, and test data for the circuit board.

This lack of communication is due to language barriers: tools come from a variety of vendors, who naturally developed their tools around their own data formats and structures. The tools work well by themselves, but not together; in moving from one step in the design process to the next, engineers usually find that the output of a tool is incompatible with the input of the tool for the next step.

To solve the problem, a consortium of electronic design automation (EDA) vendors and semiconductor vendors pooled their resources to develop a standard data format that would make it easy to exchange design information. The result is the Electronic Design Interchange Format (EDIF).

EDIF is essentially a *lingua franca* for translators. Translators can convert data files from a given design tool into EDIF as a standard format, and from EDIF into the form needed by another design tool.

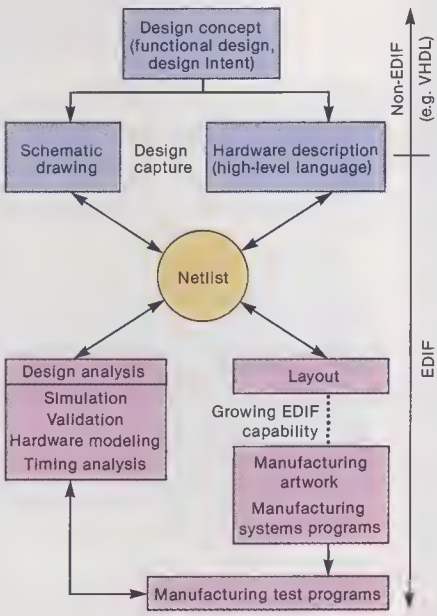
EDIF has been welcomed wholeheartedly by many electronics companies. Before EDIF, they had to improvise their own translations between tools. And if they should change vendors, they had to change tool-interface translations as well. For example, if they chose a new manufacturer of application-specific integrated circuits (ASICs), they had to install an entirely new translation program so they could present ASIC design data to the new manufacturer in the requisite form.

EDIF should not be confused with other efforts at standardization such as VHDL (VHSIC High-level Description Language); EDIF's goals and scope are quite different. VHDL describes a design at a very high level, in functional terms, while EDIF is more detail oriented. The two efforts are complementary.

John P. Eurich and Gene Roth
Engineering DataXpress Inc.

EDIF has achieved some major successes—but there are still problems to be resolved and more development to be done to make it more versatile and powerful. The consortium of developers released the first version of EDIF in May 1984. Since then, EDIF has gone through a series of revisions, and in 1988, the American National Standards Institute accepted EDIF as an industry standard. Before then, the EDIF effort had been absorbed by the Electronic Industries Association (EIA). In its current form — version 2.0.0, published by the EIA in May 1987—it is commonly used for interchanging netlists, schematic drawings, and schematic symbols between tools. It can also represent information on mask layouts, symbolic layouts, and logic models, although it is called on for these functions less frequently.

Under the EIA aegis, subcommittees are focusing on improving EDIF's abilities to represent schematic symbols and drawings. Even though EDIF 2.0.0 has become the standard mechanism for translating schematics, it still has a few deficiencies. Other subcommittees are improving EDIF's higher levels of representation. EDIF level 0 is the lowest level—level I adds formats for representing functions, constants, and parameters, and level 2 adds formats for variables and "flow-of-control" statements such as IF, THEN, ELSE, FOR, and WHILE. Still other subcommittees are breaking new ground by readying EDIF for representing printed-circuit board layout, as well as device modeling, verification, and testing. Many of these improvements will be included in the next version, EDIF 2.I.0, to be available sometime in the first half of I99I, or subsequent versions, to be available shortly thereafter.



Electronic Design Interchange Format (EDIF) tools are now available for most stages of a design effort.

EDIF, it must be said at the outset, does require substantial storage capacity. But viewed in the context of the great quantity of information that EDIF can convey, the format is highly efficient. Compared to a simple netlist, an EDIF file for the same circuit may be two, three, or even I0 times larger—but it carries added information such as properties and attributes. And the larger the netlist, the more efficient EDIF becomes in relation to it.

For a "simple" IC design of I0 000 gates, the EDIF file would be about 2 or 3 megabytes. For a more typical design, the file would be 10–I5 Mbytes. For a complete schematic of a complex IC, an EDIF file might be greater than I00 Mbytes. But here, EDIF's efficiency comes into play; with a place for everything and everything in its place, the EDIF file may actually be smaller than the original database for the schematic.

Moreover, there are ways of compressing the EDIF file. Eliminating carriage returns and white space reduces the file size by up to 50 percent. Coding EDIF keywords can reduce them from as many as 20 characters to as few as I or 2, for another 60 percent reduction in file size. Finally, there is binary compression, which can reduce the file by another 80 percent—but it, of course, can be used on the schematic database as well. EDIF files will never be as small as those in a special-purpose format, but EDIF is meant to be general purpose.

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Most ASIC vendors are just now starting to offer their customers EDIF-based translators. EDIF helps ASIC vendors broaden their customer base and, by the same token, gives customers a far wider choice of vendors. Already, almost all EDA vendors provide at least some EDIF capability. [See the accompanying list.]

Why vendors like EDIF

Vendors of design capture tools (those that interactively create schematics from the functional design), for example, provide in their products EDIF translators for schematic drawings and symbols. Vendors of design analysis tools, such as simulators, hardware modelers, and timing analyzers, offer EDIF netlist translators—EDIF can handle both "flat" netlists and "hierarchical" ones. (Flat netlists represent connectivity among primitive components, the smallest building blocks in a design—a NAND gate in a logical netlist, for example; hierarchical netlists represent connectivity among primitive and nonprimitive components of varied complexity.)

Vendors of logic synthesizers find EDIF translators for schematics and netlists an efficient means of getting design information into their systems. They find that EDIF works well for postsynthesis activities, for example, for returning a newly synthesized design to the original design-capture system for further work, and for passing the synthesized design on to tools for design analysis and implementation. And vendors of design implementation tools—such as those for laying out gate arrays, standard cells, very large-scale ICs, field-programmable gate arrays, and printed-circuit boards—are using EDIF to accept netlist and schematic files more and more.

With EDIF, customers can choose their design tools with complete freedom, to suit their particular design methods and products. They do not have to choose tools simply because they work well together, and they do not have to worry about arranging for data transfer between tools. EDIF takes care of it all.

A key benefit is that EDIF adapts readily to almost any design environment. For example, many electronics companies have their engineers develop designs on low-cost, PC-based schematic-entry tools. They find this a cost-effective way for many engineers to do design work independently on the same project. Once this initial work is done, the designs are carried, or "ported," via an EDIF link to a larger workstation-based system, where the design process is completed.

Some electronics companies have their engineers first prototype designs on field-programmable gate arrays to make sure they work before the final ASIC is designed for production. But most tools for those gate arrays are personal-computer–based, while those for ASIC design are workstation-based. Before EDIF, there was no easy way to port the design from the FPGA tool to the ASIC tool. Now, EDIF serves as the bridge between PC and workstation.

EDIF also makes it easy to move designs from one EDA vendor's workstation tool to another's. A user can mix and match workstations at will. He or she may also replace one vendor's workstation with another's and still recover the designs created on the original system. Before EDIF, users were reluctant to change vendors, despite the lure of greater efficiency and productivity, if it meant losing their substantial investment in designs.

Getting involved

Companies considering EDIF for their design systems should order the many manuals available from the EIA.

Companies that want to participate in developing EDIF should contact the EIA and ask about EDIF subcommittees. Many subcommittees are working busily on areas that will become part of EDIF in the future.

Commercial software that supports development of EDIF translators is available from several vendors [see table]. Some public-domain development software is available from the University of California at Berkeley and the University of Manchester in England.

Success stories

Sun Microsystems Inc., Mountain View, Calif., has used EDIF as a central depository format for well over a year. Sun uses EDIF translators to connect an assortment of design tools at the netlist level—tools from such EDA vendors as Gateway/Cadence, LSI Logic, Synopsis, Quad Design Technology, and Valid Logic.

To integrate its tools, Sun used the EDIF translators supplied by the vendors, but

Representative software packages with Electronic Design Interchange Format (EDIF) translators and other tools

Product	Company	Year first available	Price, US $	Platform	Operating system	Translator function/ type	Source, target	Comments
Tango-Schematic	Accel Technologies Inc.	1989	$495	IBM PC/ XT/ AT, PS/2	DOS	W/N	Sedco component libraries	Supports hierarchical or flat designs and user-definable attributes; uses third-party libraries of 1D 5DD+ parts developed by Sedco (Scotts Valley, Calif.)
Saber, Saber/ Cadat, Saber/ Verilog	Analogy Inc.	1987	$15 DDD	Sun, HP/ Apollo, DEC, Alliant	Unix, Aegis, VMS	R/N	Saber, Saber/ Cadat, Saber/Verilog (targets)	Translates EDIF into two netlists for concurrent analog and digital simulation
EDIFIN EDIFOUT	Cadence Design Systems Inc.	199D	$50DD	DEC HP/Apollo, Intergraph, NEC, Sony, Sun	Unix	RW/N, SD, mask layout	—	Supports hierarchical and flat designs
Pathfinder-TA	Computer Timing Products Inc.	1990	$5 0D0	PC, Mac	DDS, Mac	RW/N	To be determined	Netlisting is hierarchical
EDIF 2.0.D Interface	Computervision	1989	$1D DDD	CADDStation (Sun 3 and 4, Sparcstation)	Sun DS3.3, Sun OS4.0	RW/N	Both	—
EDIF Netlist Writer	Data I/O Corp.	1989	$995; $295	IBM PC, Sun 3 and Sparcstation	DOS, Unix	W/N	Future Net-5 Schematic Designer	Produces drawing cross-reference and error-report files for debugging
EDI Translator Development Environment	Engineering Data-Xpress Inc.	1987	$1D DD0+	Apollo 68K and DN 1DDDD; Sun 3 and 4; VAX/VMS, VAX/Ultrix, IBM, Mac	Domain OS, Sun DS, VMS Ultrix, DDS, Mac OS	RW/N, SD, SY	Any database or format	Is a complete EDIF translator development environment

Representative software packages with Electronic Design Interchange Format (EDIF) translators and other tools *(continued)*

Product	Company	Year first available	Price, US $	Platform	Operating system	Translator function/ type	Source, target	Comments
RUN Electronic Oesign System	formula GmbH	1989	$1750	Apple Macintosh (all models)	Mac OS A/UX (Apple Unix)	W/N	Source: RUN Electronic Oesign System Internal database Target: EOIF 2.0.0	First integrated CAE-System on the Apple Macintosh; supports hierarchical and flat designs
System HILO Logic Simulation Toolkit	GenRad Inc.	1988	$6600–$13 200	Most 32-bit Unix or VMS	Unix or VMS	R/N	System HILO EOIF interface to GHDL models	—
Edif2Ikos Netlister	IKOS Systems Inc.	1990	$5000	Sun 3 and 4; Apollo	Sun OS 4.X, SR 10.1	R/N	Source: any system that outputs EDIF 2.0 schematic or Netlist Target: IKOS 800/1900/ 2800/2900 simulation system	Supports hierarchical information
EOIF Netlist Reader 20D	Intergraph Corp.	1990	$6D00	Intergraph RISC Unix workstations	Clipper Unix (CLIX 5.3.1)	R/N	Source: any system that produces EOIF 2.0.D schematic or netlist file Target: any system that reads EOIF 2.0.0 schematic or netlist file	Supports hierarchical and flat designs
ISS IC Design Toolbox	Integrated Silicon Systems Inc.	1989	—	OEC HP/ Apollo, Sony, Sun, PC 386/486	Unix, ODS	RW/N	Source: system producing EOIF 2.0.0 schematic or netlist file Target: ISS IC Design Toolbox	Supports hierarchical designs
Logic/IC Universal Netlist Postprocessor	ISOATA Inc.	1990	$396 (PC); $792 (workst.)	OEC VAX, HP, HP/Apollo, PC, Sun 3 and 4	VMS, Ultrix, HP VX, Aegis, OOS, Sun DS 3 and 4	W/ N, SO, SY	Source: LDG/iC Gates logic synthesis for gate array implementation	—
EDIF Schematic Views	Knights Technology Inc.	1989	—	Sun 3 and 4	Sun DS 3.5, Sun OS 4.x	R/ N, SO, SY	—	—
CUPL (Universal Compiler for Programmable Logic)	Logical Oevices Inc.	1990	$2295	Sun, HP/ Apollo, OEC	OOS, Unix, VMS	CUPL: W/N, SO (for PLO design)	Source: EOIF 2.0.D netlist Target: PLO design	DnCUPL (another product) is the EOIF Netlist Translator that interfaces Schematic drawings to CUPL
EOIF Interface	Mentor Graphics Corp.	199D	—	Apollo (Sun 1991)	Unix	RW/ N, SO	Mentor Graphics design database format	Hierarchical; controlled transfer of properties
Schema III	Dmation Inc.	1985	$495	IBM PC/XT/ AT/286/386/ 486	ODS 2.0+	W/N	Schema PLO design/ selection; workstation and third-party software supporting EOIF	Schematics constructed with Schema I or II are fully compatible with Schema III
OrCAO/VST	OrCAO LP	1990	$995	IBM PC/XT/ AT/386	ODS 2.0+	R/N, SY	Source: DrCAO/SDT (another product)	Can handle 32 other netlist formats
CF30DOM	Phase Three Logic Inc.	1990	$15 000	PC and Sun	OOS, Unix	RW/N, SD, SY	Translates information through EOIF 200 to Mentor, Valid, Cadence, and other popular workstations	Schematic and translator package is also available for other popular workstations such as Valid and Cadence, and is known as CF3D00T
POM	Plessey Semiconductor	1990	$15 000	PCs, workstations	ODS 3.3, Unix	RW/N, SO, SY	Source: workst. or PC Target: ViewLogic/Silvar Lisco Systems	Accommodates hierarchical design; timing information
EOIF 200 Interface	Prime Computer Inc.	1989	$10 000	Sun 3 and 4, Sparcstation; CAOOStation	Sun DS 3.3, OS 4.0	RW/N, SO, SY	Both	—
RPM Emulation System	Duickturn Systems Inc.	1989	—	Sun 3 and 4, Sparcstation	Unix	R/N	Source: Netlist from CAE Systems; output of reader is an internal database format	Claimed as the only reprogrammable emulator supporting EDIF
EOIF I/D Netlister	Racal-Redac Inc.	1990	—	HP/Apollo 3***/4*** series, Sun 3 series	Unix System V	RW/N	Visula Oatabase	Supports hierarchical or flat designs
X-Sim System Simulation Environment	Silicon Automation Systems Inc.	1990	$20 D00	HP/Apollo, Sun, IBM, RISC 6000	Aegis, Unix, AIX	R/N	—	X-Sim is a 1076 VHOL environment with Turbo Software Accelerator
SL-Oesign	Silvar-Lisco	1990	$25 000	OEC, HP/ Apollo, Sun, Solbourne	VMS 4.7, VMS 5.2, SR 9.7, SR 10.2, Sun DS 3 and 4	RW/N, SO, SY	SL-Oesign database to EOIF v.2.0.0	Has on-line editing and netlist extraction; features multiple icon-driven windows with cross-window editing

Representative software packages with Electronic Design Interchange Format (EDIF) translators and other tools *(continued)*

Product	Company	Year first available	Price, US $	Platform	Operating system	Translator function/ type	Source, target	Comments
TASE (Test Automation Support Environment)	Simutest Inc.	1990	$15 000	DEC VAX, DEC 3100/ 5000, HP/ Apollo DN¾ xx, Sun 3 and 4, Mac U/X	VMS, Ultrix, Aegis, Sun OS, Mac U/X	R/T	Source: Daisy, Mentor, Valid, Cadence, Teradyne, GenRad; Target: Schlumberger, GenRad, Teradyne, Advan Test	—
Design Compiler	Synopsys Inc.	1988	—	DEC, HP/ Apollo, Sun, Solbourne	—	RW/N, SD, SY	Source and target: Mentor, Cadence, Valid, Daisy	Supports hierarchical design
NetTran	Tanner Research Inc.	1990	$1295	PC XT/AT/ 386/486, PS/2	DOS 2.0+	RW/N	—	Hierarchical; provides timing information, gate counts, area estimation, back annotation capacitance, timing derating
Vanguard Schematic Design System	Teradyne Inc. (Electronic Design Automation Group)	1990	$5000	DEC VAX, PC, Sun 3 and 4	VAX/VMS, DOS, Unix	RW/N	Source: Vanguard 4.1 and Vanguard 5.1; Target: any system that accepts EDIF 2.0.0	Supports hierarchical and flat designs
EDIF Netlist Writer	Valid Logic Systems	1990	—	DECstation, Sun 3 and 4	Ultrix, Unix	W/N	Source: ValidGED, ValidCOMPILER; Target: EDIF 2.0.0 Format	Supports hierarchical and flat designs
Vantage Spreadsheet EDIF Interface	Vantage Analysis Systems Inc.	1989	$10 000	Apollo, Sun	Apollo OS 10.2, Sun OS 4.03	RW/SD, SY	IEEE 1076 VHDL	Full hierarchy maintained; EDIF Read/ Write allows translation into the IEEE 1076 VHDL standard for VHDL simulation
CR 3000/SWS	Zuken America Inc.	1990	—	HP 400 Series, Sun Sparcstation	Unix	RW/N, SD, SY	Mentor Graphics design database format	Hierarchical or flat designs
Mach Tools	Zycad Corp.	1986	$15 000	HP/Apollo, Sun 3 and 4	Apollo Domain SR 10.x ; Sun OS 4.0.x	R/N, SD	—	Supports hierarchy, timing, capacitance

Key: LW=writer; R=reader; N=Netlist; SD=schematic drawing; SY=symbolic layout; T=test vectors

found it necessary to augment them with its own translators. Sun engineers, with the help of Engineering DataXpress's translator developer, wrote and tested the necessary extra software for each tool in two to six weeks. If they had started from scratch, without EDIF or a commercial translator developer, it would have taken them about six months per tool.

Unisys in San Diego, Calif., is another company that has put a successful EDIF system into service. In July 1988, Unisys decided to use EDIF as the standard method of interchange for schematics and netlists throughout the company. Like Sun Microsystems, Unisys had to develop many translators itself and employed a commercial translator development tool to speed the process and make it easier.

Besides moving netlist and schematic information around with EDIF, Unisys uses the format to back-annotate its IC designs; that is, after Unisys engineers obtain timing information on a chip design by simulation, they send it to the Unisys chip designers, who can transform the design as necessary on the basis of the more accurate timing information. The back-annotation process can be iterated with increasingly accurate timing information.

Motorola Semiconductor, Phoenix, Ariz., has been involved with EDIF from its inception, and like many other companies has made a commitment to move design information in the form of netlists, schematic drawings, and symbols. Motorola's ASIC group has developed most of its tools expressly to support EDIF. Internal engineering groups are using EDIF to interface with many of the ASIC group's tools and to tools from outside vendors. Engineering is also moving to what its members call "second generation" design and verification tools, for which they insist that vendors provide bidirectional interfaces.

Fundamental differences

On the other side of the coin, more than a few companies have run into sticky problems—most of them not with the EDIF specification itself but with the great and fundamental differences between most tools. These differences must be confronted and solved when the translation process is first set up, or else design information will be lost in transfer.

A prime example is transferring schematic information because schematic conventions vary widely among tools. For example, the rules used to determine what constitutes a connection can be quite different. One tool may consider a connection established only when the end of a line coincides with the "hot spot" (tip) of a component symbol pin. Another tool may consider a connection made if any part of the line coincides with the hot spot.

Another problem is buses. The way buses are represented graphically and connected to each other differs greatly from tool to tool. To resolve the differences, an EDIF translator must be able to modify graphics during translation. Some tools cannot even represent buses; transferring EDIF 2.0.0 bus information to such tools is difficult, if not impossible.

In some respects, EDIF 2.0.0 is incomplete. It cannot represent certain objects or concepts used in the design capture tool. An example is the For Frames concept of Mentor Graphics Corp., Beaverton, Ore., which is an efficient way of handling highly repetitive circuit elements such as those in shift registers and memories. For Frames uses a system of labels to do to all elements what it does to just one. EDIF is not yet powerful enough to capture all the information used in that tool. The For Frames problem, however, is being addressed and will be solved in the next release of EDIF.

Netlist translation with EDIF, in comparison with schematic translation, is easier. One reason is that the EDA industry shares a fairly uniform concept on connectivity, and, of course, netlists are based on connectivity. Where there are differences, resolving them is not difficult, since graphics is not involved.

Yet another knotty problem is timing information such as pin-to-pin delays and rise and fall times. Timing information is

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difficult to translate not only because different tools represent the information differently, but also because EDIF represents it in a more complex way than most translator-software writers would like to deal with. But the EDIF's creators were forced into this complexity because they wanted a format that would be comprehensive enough to handle almost any timing situation.

What's in a name?

Another problem that translator developers sometimes encounter because of EDIF's comprehensiveness is naming "objects" they use to specify a design, for example, nets, pins, and components. EDIF can easily capture the name of any object that uses ASCII characters; it places no restrictions on the length of a name or the characters in it. Most EDA systems, on the other hand, do have such restrictions; they may allow a name to be only eight characters long, for instance, or they may insist that the characters be alphanumeric only or that the second character not be an underscore. The developers of an EDIF-based translation system must take these idiosyncrasies of tools into account.

Translator developers must also handle symbol mapping on their own. For example, an initial design may be specified in a schematic capture tool by placement and interconnections of generic logic symbols. When this design description is moved to a physical design system such as a printed-circuit board layout system, it is up to the EDIF translator developers to make sure that they provide a mapping library so that the system can relate the physical components in the board layout to the primitive logic elements in the schematic.

A receiving tool will not "understand" a schematic drawing transferred to it unless the schematic symbol library on which the drawing is based is transferred, too. Symbols representing the same circuit element are usually quite different in different schematic-capture tools. If the EDA industry could standardize on a common symbol library, this transfer problem would be eliminated, but so far EDIF committees consider symbol standardization beyond their charter.

Finally, many of the problems that users have encountered with implementing an EDIF-based system are simply the result of poorly or incorrectly written EDIF translators. Unquestionably, EDIF is a complex and difficult format for the novice user. Often, translator developers will introduce their own—mistaken—interpretations into their translators and end up with translations that no tool can understand or that turn good EDIF code bad.

Developers sometimes create incorrect EDIF syntax by such errors as:

- Making up their own keywords instead of using those in EDIF's repertory. Keywords are special words, always preceded by a left parenthesis, whose meaning and use are rigorously specified by EDIF. One such keyword is "(typing form," which specifies the type of value a property, parameter, constant, or variable may have—whether, for example, the value may be boolean, integer, string, or point. Another keyword is "(joined," which is used to specify connectivity.
- Inserting properties where they are not allowed. Properties are name-value pairs (for example, "rise time 5 ns") that are made up just to hold information. They may be placed only in certain parts of the format, clearly specified by EDIF.
- Not specifying the "(typing form," such as "integer," within a property or parameter definition.
- Some translators are written so that they create schematics with empty "(joined" constructs within nets and thus do not explicitly specify connectivity.
- Other translators refer to cells in a logic file without providing the library that defines the interfaces to the cells. Still other translators are not written completely enough to handle graphic symbols or buses.

To users of these translators, it appears that EDIF does not work. In reality, it is the translators that do not work.

EDIF works

Prospective EDIF users should not get the impression that the file-interchange format is extremely difficult to place in service. Enough correctly written EDIF 2.0.0 translators are in use today to demonstrate that the format is viable for transferring schematics and netlists and that the benefits are well worth the effort.

Without EDIF to help transfer information from one tool to another, the task would be an order of magnitude more difficult. With EDIF, programmers have a common format in which to communicate. Integrating data transfer around EDIF costs far less than developing special tool-to-tool translators. EDIF has only a few problems, none insurmountable. And it can grow and adapt indefinitely.

About the authors

John P. Eurich (M) is the founder and president of Engineering DataXpress, San Jose, Calif. He has chaired the EDIF technical committee during the development of EDIF version 2.0.0. He currently directs development of data integration software based on the EDIF standard. He has a B.S. in applied science from San Diego State University in California.

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EM simulators = CAE tools

Vastly refined algorithms for finite-element analysis are putting electromagnetic (EM) simulators into the hands of any engineer who can afford a personal computer



Electromagnetic field simulation, long a specialized backwater niche, is now entering the mainstream of computer-aided engineering (CAE). Made accessible by dramatic advances in algorithms and in the PCs and workstations that run them, this technology gives electrical engineers new insights into old problems—improving their visualization and manipulation of the electric and magnetic fields that underlie all electrical products. The high reliability and accuracy of field simulation today also can be used to decrease manufacturing costs.

Field simulation allows an engineer to analyze the electromagnetic behavior of a device without building a physical prototype and taking measurements. Until fairly recently, performing such a simulation required access to a mainframe computer, a specialized knowledge of finite-element analysis (or some other technique), the patience to create the geometry and the corresponding finite-element mesh using a tedious non-graphical interface, and the ability to "see" electromagnetic fields in page after page of raw numbers.

Today, with CAE tools such as those listed in the table below, field simulation can be performed on workstations and, in simple cases, on PCs and Macintoshes. The tedious tasks of entering data and interpreting results have been transformed into pictorial form by exploiting the computer graphics interface. Using this interface, the engineer simply draws a geometric model, specifies the material properties of objects, and identifies sources of electromagnetic fields. The simulator then computes the fields that exist throughout the structure, and allows the solution to be both quantitatively manipulated and displayed on screen.

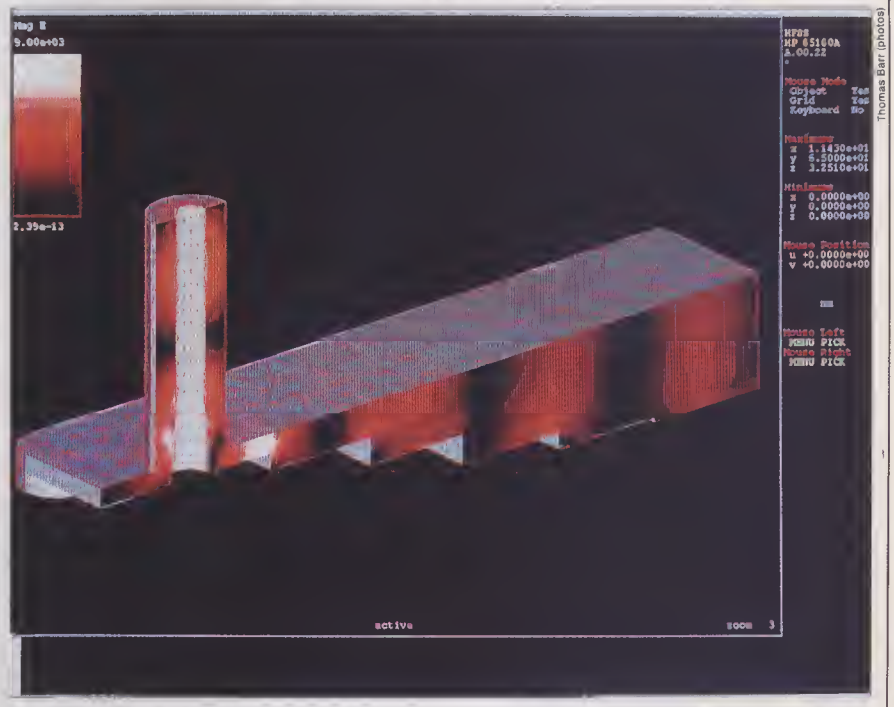
Prototypes on the screen

The challenge today is to make engineers aware of what field simulation technology can do for them. Traditional designs are formulated as one-dimensional circuits and lumped-parameter models—in terms of voltages, currents, capacitances, inductances, and so on. Electromagnetic fields, though, are not one-dimensional, but exist throughout a structure; so the precise electromagnetic behavior of a device can be predicted only when field effects are taken into account. As engineers attempt to design devices that operate at higher frequencies, that are smaller, more efficient, more precise, more sensitive, more reliable, and at the same time less expensive than ever before, the need to reckon in field effects grows steadily in importance.

The purpose of field simulation is to create reliable and accurate prototypes using a computer. The performance of the device is determined with complete reliability and with high precision by simulating the device's electromagnetic fields. These fields are fundamental to all electrical products, although few engineers in the past computed them to improve product design. The most common approach to electrical product simulation has been through the use of circuit models that, in fact, provide a high-level approximation of the electromagnetic fields. The inherent uncertainty and inaccuracy of this practice is the cause of the build-test-modify design cycle used in electrical engineering today.

The way in which simulation technology is changing the design process may be illustrated by the design of a coax-to-waveguide transition. The purpose of the transition is to convert electric signals from coaxial conductors into others for waveguides with minimum reflection.

Engineers have traditionally designed such components by estimating the impedance of each section of the transition and building a circuit model that predicts the overall transition's electrical response. But accurate values of the impedances are almost impossible to obtain and, because of the coupling of the electromagnetic field between sections, the circuit model is inaccurate even with good impedance values. As a result, building an actual pro-



Thomas Barr (photos)

[1] A three-dimensional tetrahedral mesh is used in an electromagnetic field analysis of a coax-to-waveguide transition. The field is confined to the air space within the conducting shell; its magnitude at 12.4 gigahertz along the center of the transition is shown in shades of red from dark to light. The analysis divides the space into 10 439 second-order, tangential-vector finite elements. The matrix has 52 000 by 52 000 elements. The solution is accurate to 50 decibels and took two hours when the analysis software was run on an HP 9000/834 computer.

Zoltan J. Cendes
Carnegie Mellon University

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Representative electromagnetics analysis software tools

Package	Company	Year first available	Price, US $	Platforms	Applications
Maxwell 3D	Ansoft Corp.	1989	—	Apollo, HP, IBM, IBM PC, Sony, Sun, Tektronix	Eddy currents, digital interconnects
EM-Sim	EESof	1989	—	Apollo, HP, IBM, Sun	Microwaves
High-Frequency Structure Simulator	Hewlett-Packard Co	1990	—	Apollo, HP, Sun	Microwaves
Magnet	Infolytica Corp.	1978	—	Apollo, DEC, HP, IBM PC, Sun	Electrostatics, magnetostatics, eddy currents
Magnet 2D, 3Dx	Infolytica Corp.	1978	$14 999+	Apollo, DEC, HP, IBM, IBM PC, Sun	Microwaves, particle trajectory
Coulomb	Integrated Engineering Software Inc.	1989	$17 500	IBM PC	Electrostatics 2-D/3-D
MSC/EMAS	MacNeal-Schwendler Corp.	1989	$1000–$2500 per month	Apollo, Convex, DEC, HP, IBM, Sun	Electrostatics, conduction, magnetostatics, eddy currents, transients, microwaves, resonant modes
Parasitics Parameters	Pacific Numerix Corp.	1987	$25 000	Apollo, DEC, HP, IBM, Intergraph, Sun	Digital interconnects, electrostatics, conduction
XTK	Quad Design Technology Inc.	1989	—	Apollo, DEC, HP, Sun	Digital interconnects
Greenfield	Quantic Laboratories Inc.	1986	—	Apollo, DEC, HP, Sun	Digital interconnects
EM	Sonnet Software	1989	—	Apollo, Cray, HP, IBM, Sun	Microwaves
Ansys	Swanson Analysis Systems Inc.	1970	—	Alliant, Apollo, CDC, Convex, Data General, DEC, FS Computing, Harris, HP, Honeywell, IBM, IBM PCs, Intergraph, Prime, Silicon Graphics, Stardent, Sun, Tektronix	Electrostatics, magnetostatics, eddy currents
Elektra	Vector Fields Ltd.	1990		Apollo, DEC, IBM	Eddy currents

totype has until now been essential—even though expensive and time-consuming.

Field simulation allows the performance of the coax-to-waveguide transition to be predicted to well within measured performance. The return loss predicted by field simulation for the coax-to-waveguide transition for 8.2–12.4-gigahertz values agrees with measurements at a signal level of −50 decibels. (Return loss is defined as the ratio in decibels of power reflected by the transition to the input power.) That accuracy is phenomenal: it means that 99.999 percent of input signal energy is transmitted through the structure.

Further, field simulation provides the design engineer with a tool to visualize the electromagnetic fields in the structure. A snapshot of the traveling wave in the coax-to-waveguide transition [Fig. 1] shows the magnitude of the electric field along the center of the transition at 12.4 GHz in shades of color. By studying such field patterns, engineers gain understanding of how the device works and how design changes will affect performance.

Tools for manufacturing

As for manufacturing in an integrated CAD environment, the field simulation model developed by the design engineer is passed to the manufacturing engineer. The latter then runs parameter studies of the device by varying key dimensions and materials to determine the sensitivity of device performance to these parameters. Further, the field simulation model helps determine the impact of unforeseen changes during manufacturing due to variations in supplies and facilities.

Phenomena that can be analyzed with a field simulator vary immensely. Electromagnetic fields behave quite differently at different frequencies, and engineers designing different devices are interested in different features. Those working with static and low-frequency fields are often interested in capacitances and inductances. Designers of magnetic devices are often concerned with saturation. Engineers designing connectors for high-frequency digital signals worry about return loss and the crosstalk between conductors. Those working with microwaves and optics must look into traveling waves and reflections.

As a result, certain solver modules are best suited for particular classes of problems. Commercial software is based on either the finite-element or the boundary-element method. In addition, 3-D effects predominate in some devices and require full three-dimensional analysis. Two-dimensional analysis is appropriate for axisymmetric devices and for devices in which the fields lie in a single plane. However, regardless of the particular device, analysis method, or software package, the general procedure consists of five steps: modeling, selection of materials and sources, mesh generation, solving for field values, and using these values in other calculations.

The first step in analyzing a device is to create a computer model of its geometry. Modern CAE systems use interactive graphics and solid modeling procedures to enter complicated geometries easily.

To illustrate the process, the solid model for the coax-to-waveguide converter was entered in the following way:

First, the user drew 2-D outlines of primitive shapes. For example, the waveguide component of the transition in Fig. 1 was created by first drawing the stepped rectangular outline.

The 2-D cross section was then swept or revolved through a volume of space to create a primitive solid object. For example, the length of coaxial cable was formed by sweeping its circular cross section through its length in space.

Complex features are created by uniting, intersecting, and subtracting other 3-D objects. For example, the coax-to-waveguide transition was achieved by uniting the two solids representing the coax and the stepped waveguide.

The ability to use Boolean operators (unions, intersections, and subtractions) to combine and subtract 3-D objects is critical in creating complex models. These operators are founded on the application

of the Euler invariance characteristic that states that the sum of the number of vertices and faces of a surface minus the number of its edges is constant, regardless of how the surface is divided. Using the Euler invariance characteristic automatically ensures that geometric integrity is maintained by the solid model at all times. In finite-element modeling, since material attributes must be specified for each part, it is important to distinguish true solid modeling from other methods of representing 3-D structures, such as wireframe modeling systems, in which the integrity of the attributes of each component part is not guaranteed.

Material matters

After the solid model is created, material properties such as the dielectric constant and the electric conductivity are assigned to each object in the model. Property assignment may be performed automatically by correlating object names with properties in a material database, or it may be entered via a keyboard and a panel on the screen.

Sources of electromagnetic fields also need to be specified. In the coax-to-waveguide example, the source is an input wave traveling down the coax. In other problems, quantities such as an applied voltage, the current in a coil, or a permanent magnet provide the source of the fields.

The basic idea of both the finite- and boundary-element methods is to divide the device to be simulated into a large number of small regions called finite elements and to represent either the field or its source in each element with discrete variables. For example, in the case of the coax-to-waveguide transition [Fig. 1], the electromagnetic field is confined to the air space within the conducting shell. With finite-element methods, this 3-D air space is divided into finite elements. With boundary-element methods, the mesh for only the surface of the air space is required.

Fully automatic mesh generators are now available. For 2-D models, one way to automatically divide the geometry into a mesh is to use a set of triangles called a finite-element mesh. In three dimensions, the triangle is replaced with a tetrahedron. The surface of the 3-D tetrahedral mesh used in the finite-element analysis of the coax-to-waveguide transition is shown in part at the boundaries in Fig. 1.

Since 1984, procedures based on Delaunay tessellation have become increasingly popular for finite-element mesh generation. Delaunay tessellation converts an arbitrary set of points into a triangular or tetrahedral mesh. Meshes of this kind have some very special properties: they are unique except for congruences, they may be generated efficiently by using a local refinement procedure, and, most importantly, they are optimal in that they maximize the sum of the minimum angles of all the elements in the mesh. These facts mean that Delaunay meshes avoid a problem that plagued earlier approaches—the mathematical instabilities that arise from the presence of very narrow elements. Delaunay tessellation is therefore ideal for simulation by either the finite- or boundary-element method.

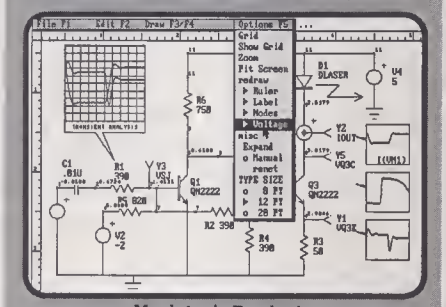
As implemented in some software packages, Delaunay mesh generation even provides the ultimate convenience of invisibility. With "invisible" mesh generation, the computer user simply enters the soli model of the device being studied, specifies its material properties, and enters "Solve." The machine then automatically creates a minimal mesh for the device, solves for the fields by using this mesh, computes the error in each element, and iteratively refines those elements having too large an error. These steps are invisible to the user, who never interacts with the mesh or even sees it unless he or she wishes to. And the simulation is guaranteed correct to within user-specified accuracy.

The solution of the coax-to-waveguide transition shown in Fig. 1 was obtained by

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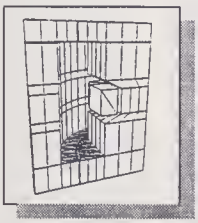
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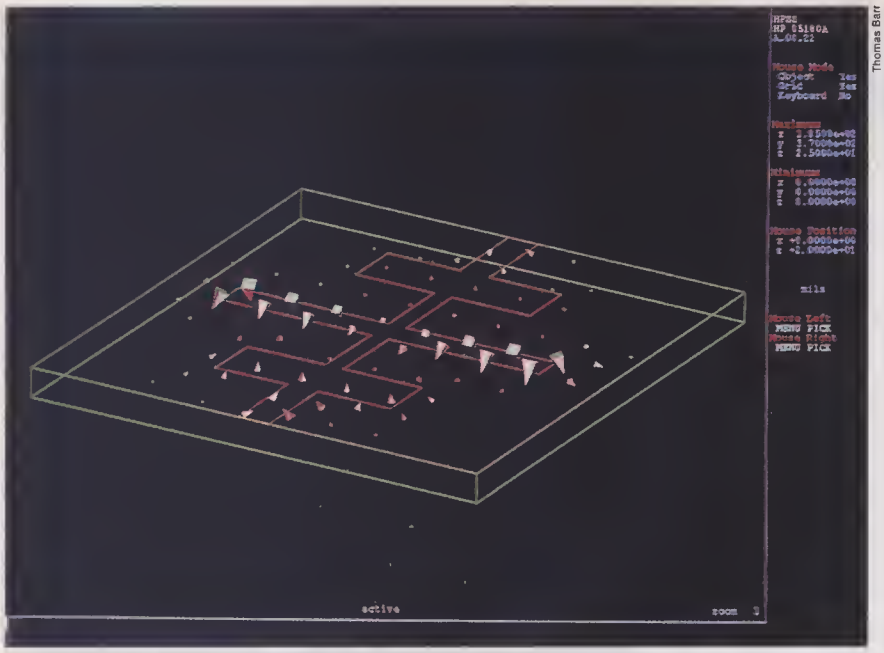
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[2] A microwave low-pass filter consisting of a printed conducting strip with three cross members on a dielectric substrate is analyzed by the finite-element method. Tetrahedrons indicate the electric field vectors at 6 GHz.

using invisible mesh generation. Eight iterations of mesh refinement were required to obtain a solution accurate to 50 dB, beginning with a coarse mesh containing 537 tetrahedral elements and ending with a fine mesh of 10 439 elements. The total solution time, including creating a solid model and eight levels of invisible mesh generation and field solutions, was two hours on HP 834 with 48 Mbytes of RAM.

The solution process

Electromagnetic field simulation involves solving Maxwell's equations, which completely describe the behavior of electromagnetic fields. The finite-element method expresses these four equations in terms of differential equations, while the boundary-element method employs integral equations. Often, to simplify the analysis, Maxwell's equations are expressed in terms of electric and magnetic potential functions.

An approximation is made of the field or potential in each element in the mesh, and the complete solution is obtained by enforcing physical and mathematical requirements on a set of local-approximation functions. These requirements are expressed as a large matrix equation that is solved for the electromagnetic field. With the finite-element methods, the resulting matrix equation is sparse, with just a few nonzero entries per row. This fact allows the matrix equation to be solved using a sparse-matrix algorithm, in which only the nonzero entries in the matrix are stored. Boundary-element methods in general produce full-matrix equations, which are very expensive and time consuming to solve. Solution times for the full matrices grow as the cube of the number of unknowns in the problem. On the other hand, the time required to solve the sparse matrices arising in the finite-element method by the preconditioned conjugate gradient algorithm increases approximately linearly with respect to the number of unknowns.

The most significant advance in finite-element methods in recent years has been the discovery that numerical electromagnetics has a complex and intricate structure that must be obeyed to provide reliable results. Traditional finite-element methods do not take this structure into account and sometimes produce spurious simulations that have no correspondence to physical reality. To grasp the numerical structure of electromagnetics, note that the continuity requirement enforced on a scalar field variable such as the electric potential is this: that the potential itself is continuous, but its derivative may jump across inter-element boundaries. On the other hand, the electric field, which is the negative gradient of the potential, satisfies a different continuity requirement: that its tangential component is continuous, but its normal component may jump across inter-element boundaries. Further, the electric flux, which is obtained by multiplying the electric field by the permittivity, satisfies a third continuity requirement: that its normal component is continuous, but its tangential component may jump across inter-element boundaries. Finally, the divergence of the electric flux is a charge distribution that is a discontinuous scalar.

Thus suppose that, in the numerical realm, the electric potential is approximated by piecewise continuous polynomials —that is, separate polynomials defined over each finite element possessing function continuity but lacking derivative continuity across inter-element boundaries. Then, to be consistent and avoid numerical instabilities, the electric field, too, must be approximated—by tangential-vector finite elements in which the approximation variables are provided by the tangential components of the field along the finite-element edges. And, in this numerical structure, permittivity is an operator that converts tangential elements into normal elements that interpolate to the normal component of the field along the finite-element edges.

Scalar, tangential-vector, and normal-vector finite elements have been derived using both first- and higher-order interpolation polynomials to represent the variation of the fields inside the finite elements. For a given matrix size, high-order finite elements yield much greater accuracy than do first-order elements. However, they require more variables per element and are much harder to program. Several current CAE programs use second-order finite element as the optimum tradeoff between accuracy and element complexity.

Although generating the field solution is an essential step in electromagnetics analysis, it is not the ultimate goal. Design issues often revolve around computing quantities such as force, torque, capacitance, inductance, saturation, heating, and energy that need to be derived from the computed electromagnetic fields.

To manipulate field quantities, many current electromagnetic CAE systems contain a calculator to perform the differentiation, integration, and vector operations required to postprocess the field solutions. The calculator operates on a stack of registers, each of which can hold an entire field quantity. The calculator usually contains separate number, line, plane, and space fields. These features make the task of performing vector calculus as easy as operating a pocket calculator. Many systems include a transcript capability by which a sequence of operations can be recorded and added to the menu as a new command. Thus a subsequent call to this command will instruct the software to perform the desired operation automatically.

To help engineers understand the electromagnetic fields in the device with which they are working, modern field simulators display plots of the electric and magnetic fields as an aid to visualization. Techniques include displaying arrow plots of vector fields, contour and shaded plots of scalar fields, and magnitude-versus-distance graphs. It is also possible to zoom into local regions and to study the field in the magnified portion of a device.

Two typical applications

The range of electromagnetic CAE applications is as broad as the electromagnetic spectrum itself. But there is only

room for two examples.

The microwave low-pass filter shown in Fig. 2 was built and measured by Hewlett-Packard Co., Palo Alto, Calif. As part of the validation of the HP high-frequency structure simulator, this filter was analyzed with the finite-element model shown in Fig. 2. A comparison of the filter's measured performance along with the results predicted by the model showed the finite-element model to be accurate throughout the frequency range from 100 megahertz to 8.5 GHz. By examining plots of the filter's electric field vector at 3, 4, 5, and 6 GHz, an engineer can observe the resonances that occur in the filter elements that produce the reflection nulls at 4 and 6 GHz. The electromagnetic coupling between stubs observed in the finite-element solution is a phenomenon not included in circuit models.

An important area for electromagnetics CAE for the future is the prediction of signal cross talk between conductors in digital circuits. As computer clock rates go higher, electromagnetic effects in the interconnects between the circuit elements become more and more important. Even today, many computers are limited in computational speed primarily by the effects of electromagnetic coupling in the digital interconnect circuits.

At relatively low frequencies (up to 100 MHz), a digital interconnect circuit will support a quasi–transverse-electromagnetic wave that may be simulated by electrostatic and magnetostatic analysis. The purpose of these static analyses is to determine the capacitance and inductance matrices for the circuit from which the signal propagation characteristics of the device may be computed. The inductance matrix is often obtained by inverting the capacitance matrix computed by setting the relative permittivities of the dielectrics equal to one in an electrostatic analysis.

Once the capacitance matrix C and the inductance matrix L for the interconnection device are found, the modes of electromagnetic signal propagation along the device are determined by computing the eigenvalues and eigenvectors of the product LC matrix. A typical interconnection system consisting of eight circular conductors and four layers of planar dielectrics has eight modes and eight velocities of propagation. The eight velocities of propagation are relatively close—ranging from 2.34×10^8 to 2.43×10^8 meters per second—but these different velocities provide different delays per meter length of line for each mode. A digital signal introduced at one end of the connector will therefore distort as it propagates along the line since it is composed of a linear combination of the eight velocity modes. Furthermore, voltages will be induced in neighboring conductors to each line since the eight voltage patterns will propagate along the conductors.

To provide a specific example of crosstalk and pulse distortion, the eight conductors in the connector were connected at each end and a pulse was applied to the input end of the first line. Crosstalk on the second line is induced directly by the input signal on the first and is reduced in magnitude but exhibits no distortion. A second signal, however, is caused by the input wave propagating down and back along the connector and is badly distorted by the dispersion of the eight propagating modes.

The signals predicted by finite-element analysis and mode propagation are remarkably close to the measured values. The simulation catches even small dips in the distorted signal that might have been ascribed simply to noise on the line. This demonstrates the power of electromagnetic CAE: even the noise that electrical engineers have tried to avoid for decades is in reality an electromagnetic effect that can be accurately and completely modeled by solving the electromagnetic field equations.

Software pointers

While many electromagnetics CAE software packages are available, their ranges of application vary greatly. It is therefore imperative to investigate the suitability of the software to each application. In general, software tuned to a particular area will be easier to use in that area than general-purpose software that tries to be all things to all people. Most software is available on a one-month-trial basis. It is a good idea to try out several packages before deciding on the one to purchase. Also, note that it takes at least one to two months to become proficient with this type of design tool.

The following capabilities should be considered in selecting electromagnetics CAE software:

General issues

• Ease of use. Some software packages date from the remote computer era when data was entered as card images, while other software was developed with computer graphics, pop-up menus, and data panels in mind. In general, a graphics-oriented interface that employs menu commands selected by a mouse simplifies program operation and makes you more productive more quickly.

• Quality. How completely is the software tested on the range of problems for which it is designed? How responsive are the customer support personnel if there is a problem? Customer support is a two-edged sword: you need to have it there, but you do not want to get to know the staff support personnel on a first-name basis. Be leery of a company that promotes the size of its customer support staff over the quality and ease of use of its software.

• Integrity. Is the user interface consistent throughout the entire simulation process, or are different systems used for problem entry, for analysis, and for postprocessing?

• Documentation. How good is the user's manual? Are there tutorial manuals and example problems that can help you to get started?

• Flexibility. This is also a two-edged sword. On the one hand, you want the software to work with the full range of problems in which you are interested. On the other hand, getting a too-general package can lead to unnecessary complications.

• User training. Are courses in the use of the software available, and are they designed to address the type of problems that you have?

• Hardware. Does the software run on a variety of platforms ranging from inexpensive PCs and workstations to high-performance supercomputers?

Problem definition

• CAD interfaces. Do easy-to-use interfaces to CAD programs and to other analysis packages exist?

• Geometry entry. Is the problem geometry entered via simple solid modeling commands, or must it be built up piece by piece?

• Parametric dimensions. Does the software support parametric dimensions that make it easy to make design changes, or does it require reentering the geometry if there is a change in the problem dimensions?

• Data entry. Is there a material database that sets material attributes automatically? Does the software employ pop-up computer graphics panels for ease of data entry?

• Grids. Does the software provide user-defined grids with snap-to-grid-point or snap-to-object-point capability that ensure crisp drawings with parallel lines that are truly parallel and conforming objects that match perfectly?

• Lists. Can groups of objects be assigned to a single list so that a whole group of objects may be manipulated independently of the other objects in the problem space?

• Views. Can objects be split and fields viewed along user-defined planes?

• Interaction. Does the software provide the capability to "touch" the model by pointing on the computer graphics screen with the cursor and mouse to obtain coordinate information directly?

Analysis

• Mesh generation. Is mesh generation invisible or must it be performed by the user? If the latter, is it more or less automatic, or does it require a great deal of user knowledge and interaction?

• Error estimates. Does the software provide error estimates for the computed solutions?

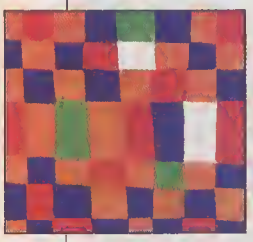
• Spurious solutions. How are the spurious solutions inherent in ordinary finite elements detected and eliminated?

• Sparse-matrix procedures. Are efficient sparse-matrix solution procedures (such

(Continued on p. 93)

The case for CASE tools

Software now being embedded in everything from electronic credit cards to mission-critical flight systems is creating a demand for CASE tools for all phases of the software's life-cycle



Spectrum *staff*

Just about every electronic system being engineered today contains software. That was not the situation in the 1970s, when electrical engineering meant designing hardware and when the focus of design was the creation of circuitry. Today, a typical engineering team often comprises two software designers for every engineer who is working on hardware.

The dependence of products on software is thus a relatively new phenomenon, and one with which the electronics industry is just beginning to come to grips. Whereas engineers have had tools to measure the performance of hardware and the course of its development for most of the 20th century, they are just starting (comparatively speaking) to develop and employ tools that will give them the same degree of control over software development. In fact, it was not until the mid-1980s that an umbrella term for this effort—CASE, or computer-aided software engineering—was coined.

Of course, software was being created long before. In the early 1950s, the first commercial computers begot a need for people who could make them perform numerous accounting tasks: billing, record keeping, and so forth. Then, too, scientists were employing mainframe computers to make complex calculations for both military and civilian projects. During this period, the first computer languages, Cobol (Common Business Oriented Language) and Fortran (Formula Translation), were developed.

These high-level languages reflect the fundamental benefits of CASE tools: they allow a programmer to work at a higher level of abstraction, concentrating on the problem that the software must solve, rather than on how the hardware uses 5-volt or 0-V signals. They thereby make the programmer more productive and allow others to understand what he or she is doing and even join in creating software.

When a user wants to run a program written in a high-level language, having the computer interpret that program one line at a time into the 1s and 0s it understands slows it down. Therefore, compilers were developed to convert an entire program into machine-readable code before the program was run. Debuggers were developed to allow programs to be checked for adherence to programming rules before they were run, and editors were created to enable programmers to correct their mistakes. Linkers allowed programs to be written in modules and joined together so that they would work as a single entity. And monitor tools were developed so that software developers could see how efficient their programs were.

With the advent of the microprocessor, software became a standard part of most electronic products. Companies therefore needed to organize the process of software development so that embedded software—code that is invisible to the ultimate user but that gives the product its functionality—could be created on schedule. They began to employ strict software methodologies, using methodology companions that assisted the programmer and made sure that he or she followed the method.

They also began to use suites of software tools that worked well together. New languages (Pascal, C, and C^{++}) that made programming more organized and operated more efficiently with popular computer operating systems were developed. The U.S. Department of Defense evolved an all-encompassing development and maintenance environment called Ada.

Future CASE

Today, CASE is beginning to extend its reach beyond software generation—the term is coming to stand for "computer-aided systems engineering." Developers are working on tools that will let companies capture the basic concepts behind a design and simulate the concepts so that potential customers will be able to "fly before buy." They are creating "virtual realities" in which software so mimics the real world that the simulation and reality are "virtually" indistinguishable.

Further, CASE companies are looking at ways of helping design managers decide what should be done in hardware and what in software, and what kinds of hardware and software should be employed. Other tools are being created to control development and check progress against the design goals, once they have been decided upon. The ultimate objective is for hardware and software designers, manufacturing engineers, logistics and maintenance support personnel, and even documentation specialists to be able to perform their respective project tasks in parallel—a development being referred to as concurrent engineering.

Software engineering today

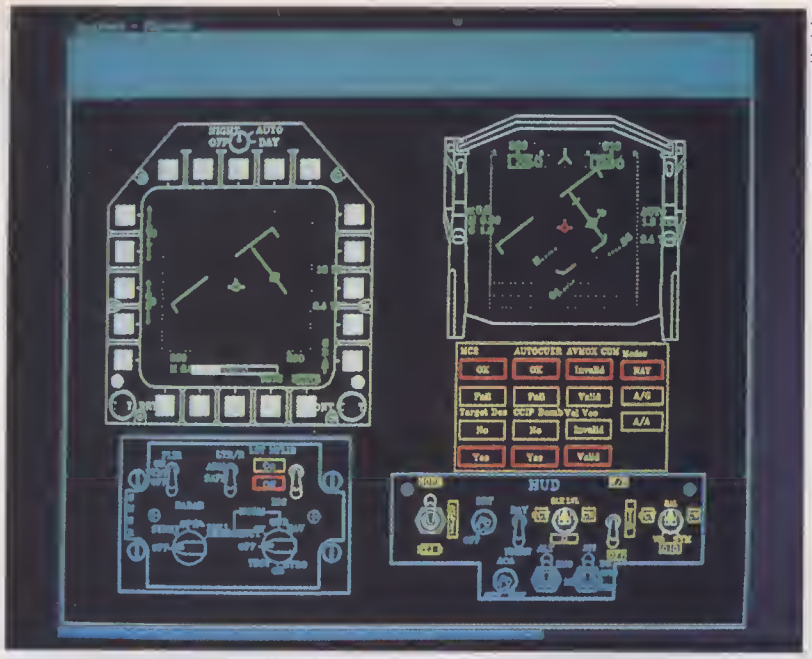
The lessons learned from the historical development of software engineering have led to an organized approach to software development today. No longer do programmers simply go off and write code (although there are some who would still prefer to do so). In CASE, the programming organization takes a top-down approach to creating software, much as hardware designers take a top-down approach to system design.

A modern software project begins with a project/product planning (P/PP) phase in which a specification is generated. Ideally, the specification puts into unambiguous terms exactly what the software should accomplish. Basic decisions about what language or languages and tools will be needed for the project are usually made at this time. At this point, CASE tools can provide help in organizing, documenting, and generating a specification. Further, with simulation tools, the team can mock up the software system so that the potential users interact with it and critique it.

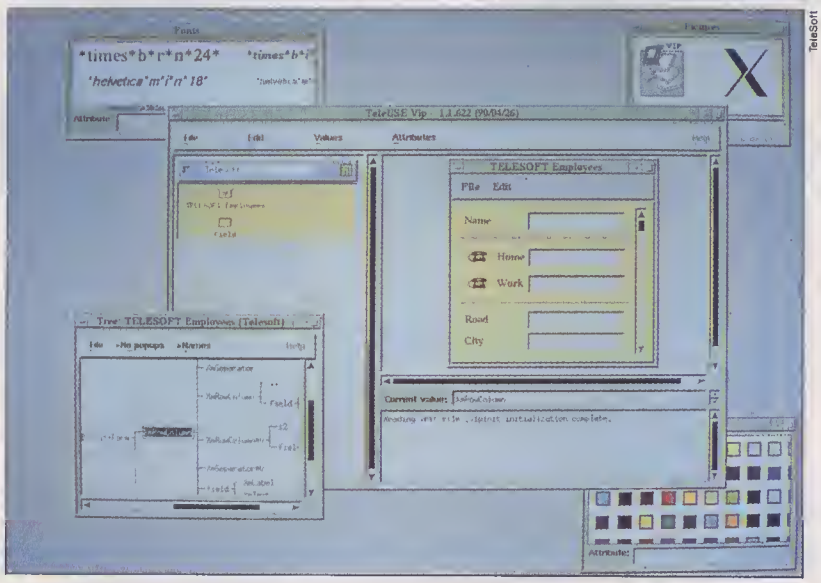
Once agreement has been reached on what the software should do, the team can create an architecture for the system, which they do during the requirements/design analysis (R/DA) phase. In creating an overall architecture, the proposed software system is divided up into programs, routines, and subroutines and the interdependencies of these modules is clearly delineated.

For example, an editorial software system can consist of several programs that interact; not only would there be a word capture system, but there could also be dictionaries for checking spelling, a thesaurus for finding synonyms, and perhaps a grammar checker. These programs would have several routines. The dictionary program would have a routine that allows the user to select a particular dictionary or to create a special dictionary. The dictionary

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i-Logix Inc.



TeleSoft

CASE tools help throughout the software lifecycle. During software systems definition, simulating the system (such as that for cockpit instrumentation, top) helps developers find out from potential customers if they are on the right track. For the implementation of a user interface (see bottom), CASE tools can let the programmer concentrate on the appearance of the interface, which would be far from apparent in its code.

would also have subroutines checking the spelling of a word and for replacing a misspelled word.

In creating an architecture, the software developers can see what routines and subroutines may be used in several places in the system. Further, they may be able to identify areas that can be implemented by using code previously created for another project. One of the major goals of CASE is to reuse existing code, thereby minimizing the effort needed to create new systems.

Having defined the architecture, the team is now able to concentrate on how various functions should be implemented. During this software design (SD) phase, the focus is on finding or creating the algorithms that must be encoded to implement the various software tasks.

Lower CASE

Defining algorithms completes the effort in what is called the Upper CASE part of the design. What follows, Lower CASE, is the true production of the software system. The first effort in Lower CASE is to take the algorithms that are the output of the SD phase and put them into code, that is, what is generally called programming. During SD, programmers will use editors, compilers, and such to create the actual programs.

Their efficiency will depend primarily, however, on the language in which they work. A programmer working in an assembly language can usually produce only one line of good code per hour, whereas a C programmer may produce 20 lines in the same time. The choice of languages for particular modules of code is generally based on how quickly the code must run; assembly (which interacts directly with hardware) executes much more quickly than, say, Fortran. One reason that C is very attractive is that, while it is a high-level language, it generates very efficient code and allows access to a machine's hardware.

As code is being created, management would like programmers to document their effort so that others can understand what the code is supposed to do and how it does it. Using a structured technique makes it easier for others to understand code, and it is also necessary that programmers add comments to the code to make it clear.

At the same time, documentation tools are needed to provide potential users with a guide to the software's operation. If this can be done in parallel with the generation of the software, the software and documentation will be ready for release sooner than if the documentation process begins only after the software is complete and programmers have gone on to other tasks.

Documentation is also needed so that others can maintain and update software once it has been released. Part of the software maintenance effort is keeping track of which modules have been used to create a version of the software, while another part is determining the cause of a software failure. For the latter function, the tools used are often the same ones used when hardware and software are integrated. However, they are applied differently.

For example, during hardware and software integration (H/SI), engineers may use profilers to see how efficiently a particular module runs in the hardware system. If they do not like the result—that is, if the module takes too long to run—they may go back and recode the module to make it more efficient; they may even decide to write the code in assembly rather than in a high-level language. For software service, maintenance personnel might profile a software operation to see how each module is performing, and use the resulting data to look for the source of a fault.

Methodologies

As noted earlier, CASE methodologies take programmers away from the "let's just write code" school of programming. Programmers now talk of various ways in which they can approach the problem of creating a system and the roles of the various elements that make up programs.

The earliest attempt to systematize program generation is attributed to Edsger Dijkstra, who is sometimes called the father of structured programming. Originally called "GOTO-less programming,"

Representative computer-aided software engineering (CASE) packages

Package	Company	Year first available	Price, US $	Platform	Operating system	Tool function
IPSE	Atherton Technology	1987	$15 150	VAX, RS/6000, Sun	AIX, Sun OS	Project management
ADAS	Cadre Technologies Inc.	1988	N.A.	VAXstation, OECstation, HP/Apollo, HP 9000, IBM RT, Sun	Domain OS, Sun OS, Ultrix, Unix, VMS	System simulation
Drganized C	Code Farms Inc.	1989	$75 (DOS), $12 745 (Unix), $20 000 (full source)	PC; Sun 3, 4, Sparcstation; Sony (News), HP 9000, VAX, MIPS, others	DOS, Unix, VMS	Oata management
C++/SoftBench	Hewlett-Packard Co.	1990	$9995	HP/Apollo, HP 9000	Domain OS, Unix	Programming environment
Statemate	i-Logix Inc.	1987	$75 000	DECstation, VAXstation, HP/Apollo, Sun	Aegis, Domain DS, Sun OS, Ultrix, VMS	System definition
Software through Pictures	Interactive Oevelopment Environments (IDE) Inc.	1984	$5000–$21 000	DECstation, VAXstation, HP/Apollo, HP 9000, RS/6000; Sun 2, 3, 4, Sparcstation, 386i	AIX, Sun OS, Ultrix, Unix, VMS, MPUX, Domain DS	Integrated environment
Eiffel	Interactive Software Engineering Inc.	1985	$3000 (avg.)	Sun, Sony, IBM, Data General, DEC, HP/Apollo, MIPS, HP, Silicon Graphics, Sequent, Pyramid, Amdahl, Apple A/UX	AIX, A/UX, HP-UX, Sun OS, Ultrix, DG-UX, SCO Open Desktop, ESix, 389ix, BSD 4.3, UTS, News OS 3.3, VMS	Programming language and environment
CASE Station	Mentor Graphics Inc.	1990	N.A.	HP/Apollo, Sun	Aegis, Domain DS, Sun OS, Unix	Integrated environment
Design/IOEF	Meta-Software Corp.	1987	$2995	PC/AT, PS/2, Macintosh	DOS/Windows, MAC OS	Methodology companion
NDP Fortran	MicroWay Inc.	1987 (386)	$895–$1995 (depending on platform)	PC 386, 486, i860	OOS, Unix, Xenix, Sun OS	Compiler
OPNET	MIL 3 Inc.	1987	$14 000	OECstation, HP/Apollo, Silicon Graphics, Sun 3, 4, Sparcstation	Ultrix, IRIX, Domain OS, Sun OS	Network and system simulation
NeuralWorks Professional II	NeuralWare Inc.	1987	$1495 (PC, Mac); $2995 (Sun); N.A. (NCube)	PC, Macintosh, Sun 3,4, 286i; NCube	DOS 3.X, MAC OS, Sun OS 4.0.1, AXIS OS plus Vertex MSG ROUT	AI neural network development environment
Objectivity/DB	Objectivity Inc.	1990	$15 000	Sun, DECstation, VAX, IBM RS-6000	Sun OS, Ultrix, VMS, A/IX	
Janus/Ada CASE	RR Software Inc.	1990	$8750	PC 386, Sun	OOS/Windows, Unix/X-windows	Ada design environment
Saber-C	Saber Software Inc.	1987	$2995	DECstation, VAXstation, Sun	Sun DS, Ultrix	Programming environment
SES/workbench	Scientific & Engineering Software (SES) Inc.	1989	N.A.	VAXstation, HP/Apollo, Sun	Unix, VMS	System design and simulation
CCC	Softool Corp.	1977	N.A.	IBM 30XX, 43XX, 9570, VAXstation, OECstation, HP 9000; Sun 3, 4; Data General, Concurrent, PC, others	MVS, VM, Ultrix, HP-UX, Unix, MPX, VTX, DOS, OS/2, others	Change/configuration control
Software TestWorks, "stw"	Software Research (SR) Inc.	1986	$5000–$25 000 (depending on platform, composition)	HP/Apollo, HP 9000, PC286, 386, PS/2, RS/6000; Sun 3, 4, Sparcstation, 386i	AIX, Oomain DS, DOS, HP-UX, OS/2, Unix, Xenix	Software test
Model-C	System Control Technology Inc.	1988	N.A.	VAXstation, Sun 3, Sparcstation	VMS, Unix	System simulation
T3	TCI Software Research Inc.	1985	$595	PC	DOS	Technical documentation
TeleUSE	TeleSoft	1990	$7500	DECstation, Aviion, Sun 3,4,	Sun DS, Ultrix, Unix	Graphical interface design environment
IEF	Texas Instruments Inc.	1987	N.A.	PC/AT, PS/2, IBM, OEC, Tandem	OOS, OS/2, VM, VMS, MVS, Unix	Integrated environment for information engineering

Activities supported							Methodology				
P/PP	RD/A	SD	SI	SM	SDOC	H/SI	IO	PO	DO	SP	Comments
●	●	●	●	●	●		●		●	●	None
●	●					●	●	●		●	None
●		●	●	●			●	●	●	●	Works in C and C++, either for in-code data or as a database maker; library of persistent data objects; automatic change control
		●	●	●	●					●	None
●	●						●				None
●	●	●	●	●	●	●	●	●	●	●	None
		●	●						●		None
	●	●	●	●	●		●	●	●	●	Control-panel and algorithm prototyping
●	●	●			●			●	●		Companion for structured analysis and design technique (SADT); allows creation of graphical executable models
			●							●	None
●	●	●						●			None
			●						●		None
											None
●	●	●	●	●	●					●	None
			●	●		●	●	●	●	●	None
●	●	●	●			●	●	●	●	●	None
●	●	●	●	●	●	●	●	●	●	●	Cross life-cycle support
		●	●	●						●	Includes TCAT, STCAT, SMARTS, EXDIFF, CAPBANK, TDGEN, and TCATPATH packages for test software generation
	●		●	●	●						None
●	●				●						None
		●	●	●				●	●		None
●	●	●	●	●	●	●	●	●			Graphical interface, full life-cycle support

structured programming advocates the modularizing of code and following a rigorous, checklist approach to code generation.

Among Dijkstra followers, Tom DeMarco and Edward Yourdan refined their mentor's approach to a highly systematized one in which all turns on understanding the flow of data through various processes. Their approach, referred to as the data-oriented or Yourdan-DeMarco methodology, makes extensive use of data-flow diagrams, in which various operations are represented as circles, and a path between them indicates how data from one operation flows into the next.

A natural outgrowth of this approach for many programmers is to concentrate on the procedures, and to see programming as the process of implementing procedures; hence adherents to this methodology call it procedure-oriented (PO), and work at creating the most efficient procedures without concern for the kind of data being processed.

Other programmers, however, have taken to looking at the relationships between data, seeing the relationships as what is truly information. In this information-oriented (IO) approach, lists of data and the interrelationships implied in these lists is the primary focal point. The field of expert systems, with its emphasis on heuristics, is a prime example of information engineering.

Object-oriented programming (OOP) is also an example of an approach in which the relationships between data types, called objects, is the primary focus. Most proponents of OOP will stress that it is not a structured programming approach, at least in the sense of the requirement to follow strict programming practices. However, in the process of creating object-oriented programs, it is fundamentally necessary to define the relationships between data; hence in the resultant programs, there is a very strong structural relationship, one that is clearly defined. The nature of this structure, however, is usually not predetermined, but is an outgrowth of the programming process. ◆

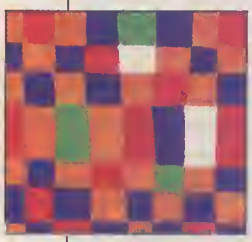
KEY

Activity supported
P/PP = project/product planning
RD/A = requirement design/analysis
SD = software design
SI = software implementation
SM = software maintenance
SDOC = software documentation
H/SI = hardware/software integration

Methodology
IO = information-oriented
PO = procedure-oriented
DO = data-oriented
SP = structured programming

Board tools proliferate

Software for the design of printed-circuit boards is becoming a common part of every engineer's workplace, permitting better designs from the start



No longer confined to mainframe computers or mechanical drafting departments, the printed-circuit board layout has moved into the world of personal computers and workstations. With that move, board design has become the province of mainstream electronics engineers, as another function is added to the IC- and system-design repertoire.

Running the gamut from basic entry-level PC packages selling for under US $1000, to full-fledged workstation-based tools, printed-circuit board products offer an amazing range of capabilities. Not quite "plug-and-play" offerings yet, they are getting close. Although the most critical or complex layouts still need human judgment and intervention, the trend is toward automatic placement of components and autorouters, which automatically set the traces once components are in place.

However, manual placement and routing, especially with entry-level software, remain the leading methods. Answering the objections of those who say that autorouting cannot produce the most efficient layout in all cases, some autorouters are interactive, allowing the engineer to interrupt the automatic process and intervene to change critical paths as necessary.

The tables that follow are a representative sampling of the hundreds of available commercial software packages, and offer only a brief glimpse at the capabilities of those listed. A comprehensive evaluation would include a host of parameters and features too numerous to list: routing methods and strategies, editing capabilities, design and error rule checking, printer and plotter support, and all of the options involved in good board design–pad configurations and sizes, isolation of elements, the kinds of vias handled, the size and resolution of grids (both manual and autorouted), solder mask and silk screen capabilities, and so on.

With circuit speeds soaring, other factors should be considered. Beyond about 35 megahertz, standard printed-circuit board traces may act like transmission lines, and microstrip and stripline designs

Spectrum *staff*

1. Printed-circuit-board positioning and layout packages* *(see footnotes, p. 84)*

Package	Company	Year first available	Price, US $	Platform
Tango-PCB PLUS	Accel Technologies Inc.	1988	$995	IBM PC/XT/AT, PS/2, and compatibles
Tango-Route PLUS	Accel Technologies Inc.	1988	$895	IBM PC/XT/AT, PS/2, and compatibles
Associate Designer	Cadam/P-Cad	1986	$6200	IBM 286/386 and compatibles
Master Designer	Cadam/P-Cad	1987	$15 000	IBM 286/386 and compatibles
Premier PCB	Cadam/P-Cad	1990	$20 000	Sun Sparcstation, IBM RISC System/6000
Amadeus/Prance	Cadence Design Systems Inc.	1988	—	DECstation 2100, 3100, 5000, Sun Sparcstation 1+
HP PCDS	Hewlett-Packard Co.	1986	$14 000–$40 000	HP 9000 workstations
Board Station 1985	Mentor Graphics Corp.	Updated 1990	$85 000	HP/Apollo, Sun
PCB II	OrCAD Systems Corp.	1990	$1495	IBM PC/XT/AT, PS/2, and compatibles
MAXI/PC	Racal-Redac Inc.	1988	$995	IBM XT/AT/386, PS/2
CADSTAR Professional 1987	Racal-Redac Inc.	Updated 1990	$4850	IBM AT/386, PS/2
Bravo3	Schlumberger CAD/CAM	1987	$8500	DECstation, VAXstation
Vanguard PCB layout 1986 Licensees	Teradyne EDA	1986	$9500	Sun 3/4, VAX, PC 286/386, and compatibles
Vanguard Autorouter 1988 Licensees	Teradyne EDA	1988	$5000 (PC); $12 000 (workst.)	Sun 3/4, VAX, PC 286/386, and compatibles
Allegro PCB Design System	Valid Logic Systems	1987	$50 000	Sun, DEC, IBM
HiWIRE II	Wintek Corp.	1990	$995	IBM PC/AT, PS/2, Compaq, and compatibles

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may replace standard traces. Trace-contributed cross talk, delays, overshoots, ringing, and the like may become important factors. Because certain paths may become critical to overall performance, they must also be identified. Responding to that need is a growing host of point tools—software that specializes in identifying problems caused by transmission-line and electromagnetic-coupling effects.

Some of those tools are listed in the tables. Many more are available, as are countless specialized tools for, say, microwave and radio frequency (RF) design simulation or auxiliary functions. Many carry industry-standard interfaces, and so can work with a variety of other computer-aided design (CAD) and layout software.

One example of a specialized tool is Academy, a framework and graphical interface for microwave and RF simulations from EEsof Inc., Westlake Village, Calif. Also offered by EEsof is LineCalc, a transmission-line analyzer. Another example is Pro-Elec, from Applications Development in Metairie, La.; it is a CAD drawing environment that contains an extensive symbol library. Infolytica Corp. of Montreal, offers MagNet, a finite-element analysis program that specializes in electromagnetics and electrostatics.

The tables are a broad-brush listing of some of the more salient characteristics of commercially available layout and analysis packages. Generally, those packages that tap the power of workstations offer

Operating system	Performance[1] (max. board size, no. of layers, component count; min. grid spacing)	Layout types	Libraries	Comments
DOS	32 x 32 in.; 23 layers; EICs virtually unlimited within design, EMS support; 1-mil grid to signal and power/ground planes	Through-hole and double-sided SMT; both sides fine-line	Standard through-hole, SMT patterns; graphical new-part creation	Manual and auto place; design-rule check; photoplot file viewer; force vectors; DXF; PostScript
DOS	10 layers; EICs virtually unlimited within design, EMS support	5 grids, 10–25 mils with off-grid capability, fine-line	—	Single-grid, four-layer autorouter for PCB and PLUS version; multipass algorithms; 90- and 45-degree routing; PLUS versions: fine-line, 5 grids of 10–25 mils
DOS	60 x 60 in.; 100 layers; 500 components; 1-mil grid	SMT, flex circuits, analog, digital, hybrid	6000 parts (TTL, CMOS, ECL, discretes, linear; Intel, Motorola)	Manual and auto place-and-route; maze and rip-and-retry algorithms
DDS	60 x 60 in.; 100 layers; 2500 components; 1-mil grid	SMT, flex circuits, analog, digital, hybrid	6000 parts (TTL, CMOS, ECL, discretes, linear; Intel, Motorola)	Manual and auto place-and-route; maze and rip-and-retry algorithms
Unix, AIX	Unlimited board size; 100 layers	SMT, flex circuits, analog, digital, hybrid	6000 parts (TTL, CMOS, ECL, discretes, linear; Intel, Motorola)	Manual and auto place-and-route; maze and rip-and-retry algorithms
Ultrix, Sun OS	64 x 64 in.; 32 layers; no limit	Multilayer; double-sided SMT; high-speed logic	Integrated library with Amadeus tools (TTL, ECL, and high-speed logic)	Warp grid concept combines best of gridded router technology with gridless capability
HP-UX, X-windows	45 x 45 in.; 128 layers; unlimited components, grids, apertures	SMT, digital, mixed-analog/digital, thick-film hybrid	9000 parts standard; user-specific creation	Interactive operation on either side, off-grid routing, auto breakout generation
Domain DS, Sun OS	100 x 100 in.; 255 layers; 32 000 components	Double-sided SMT; through-hole, flex circuits; analog/ digital, mixed hybrids, MCMs, Multiwire panels	ECL, CMDS, TTL, high-speed logic; PLOs, memory, logic automation models; over 2500 analog parts	Full-fledged package integrated with other EDA tools; common database includes auto-schematics, simulation, manufacturing tools (Sun, etc.)
DDS, OS/2	32 x 32 in.; 16 layers; 270 EICs; 1-mil grid	Double-sided SMT; analog/digital	300 modules	Interactive manual autorouting on grids of 5, 10, 20, 25, 50, 100 mils (manual down to 1 mil)
DOS	32 x 32 in.; 16 signal layers; 250 EICs, 1023 components; 1-mil grid	Double-sided SMT; analog/digital	1200 parts standard, 20 000 parts optional from Sedco libraries	Entry-level package; 5500 signal connections
DOS	32 x 32 in.; 16 signal layers; 600 EICs, 1023 components; 1-mil grid	Double-sided SMT, buried and blind vias; analog/digital	1200 parts standard, 20 000 parts optional from Sedco Jedec/IEEE libraries	Midrange package, advanced positioning and layout, advanced autorouter, 650–5400 connections
VMS, Ultrix X-windows	No limitations on board size, layers, grid	Double-sided SMT	300 components arranged by package type	Interactive or automatic electromechanical integration; 3-D solids modeling, wireframes
Sun OS, VMS, DDS	32 x 32 in.; 256 layers (any use); 1800 (PC) and 5000 (workstation) components; 1-mil grid	Through-hole, double-sided SMT, buried and blind vias, fine-line	130 footprints used with 5000 schematic symbols	Full multiwindow schematic integration, autoplace, DRC, Gerber, Excellon
Sun OS, VMS, DOS	32 x 32 in.; 30 layers; 1-mil grid	Through-hole, double-sided SMT, buried and blind vias, fine-line	130 footprints used with 5000 schematic symbols	Simultaneous routing any repeating pattern grid; fast 100% rip-up-and-retry routing; nonstandard devices and grids; state-of-the-art routing on PC and workstation
Unix, AIX, VMS, Ultrix	48 layers; unlimited components	SMT, MCMs, hybrids, high-speed, mixed ECL/TTL	7000 components	Auto placement, test preparation, routing, in-process electrical analysis, postprocessing, third-party database translators
DOS	60 x 60 in.; 255 layers; 200 EICs; 1-mil grid	Through-hole; SMT	2500 components, users customize own components; ECL, microstrip, others	EICs in 640K, supports LIM and XMS memory; optional autorouters; 100% completion, gridless, rip-up-and-reroute on all layers

commensurately more layout power: larger boards, more connections and components, speedier layout, and more features. But PC-based tools are becoming more facile; the edges are blurring as it becomes harder to distinguish between high-end personal computers and low-end workstations.

As with any complex product, measurement of performance usually is not so simple as specifying a figure, or figures, of merit. Layout speed is especially hard to pin down. That number—somewhat analogous to that derived with computer benchmarks—depends greatly on the conditions selected for the "run." Nevertheless, most circuit board software lists limitations in board size, components and connections, number of layers, and so on. In the end, the actual application will dictate a specification's significance.

Many, if not most, of the available packages are not meant to be stand-alone tools, but work in conjunction with other major computer-aided engineering (CAE) tools—schematic capture and simulation software, for example. Consequently, some packages come with those capabilities attached, others offer them as options, and still others are integrated into a complete CAE environment, including the workstation. In most cases, however, some kind of electrical and design-rule checking is standard fare. ◆

2. Printed-circuit-board analysis packages*

Package	Company	Year first available	Price, US $	Platform
XTK Crosstalk toolkit	Quad Design Technology Inc.	1989	$17 000–$62 000	Sun, HP/Apollo, DEC, MIPs, IBM, Convex
Greenfield	Quantic Laboratories Inc.	1983	$9600–$50 000	Sun, HP/Apollo, Intergraph, DECstation, MIPs
BoardScan	Quantic Laboratories Inc.	1990	$9500–$14 000	Sun, HP/Apollo, Intergraph, DECstation
Swiftline	Swiftlogic Inc.	1990	$12 500	Mentor Graphics, HP/Apollo
Swiftnoise	Swiftlogic Inc.	1988	$12 500	Mentor Graphics, HP/Apollo
Allegro Signal Noise Analysis	Valid Logic Systems	1989	$15 000	Sun, DEC, IBM

1 1 in. = 1 inch = 25.4 millimeters; 1 mil = 25.4 micrometers
2 Output reports can be sorted by reflections, cross talk, thermal shift, noise margin, or all violations. In an on-line mode, re-analyzes the effects of a change to the database model and presents them as millivolts of noise within the circuit.
*Abbreviations are spelled out in "Defining terms," p. 48.

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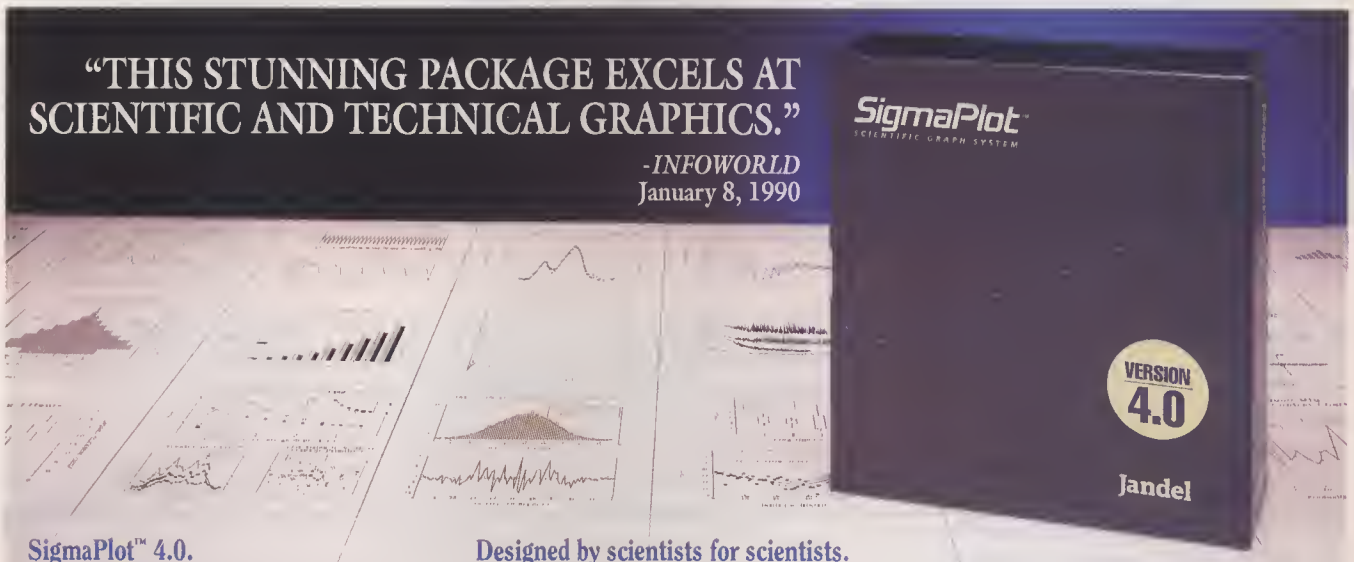
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Circle No. 206

Operating system	Analysis method	Results display	Libraries	Comments
Unix, Aegis, DOS	Conformal-mapped/ finite-element field solution; direct solution Eigenmate propagation	Waveforms and delays, cross talk and signal quality reports	Fast models for TTL, CMOS, ECL; models for some RAM, ROM, micro-processors	Includes transmission-line calculator, other tools
Sun OS, Aegis/Domain OS, HP-UX, CLIX, Ultrix, Unicos	Boundary-element, modal, sparse-matrix analyses simulate complex networks, transmission lines	Tables, waveforms, skin effect vs. frequency, cross talk, ringing, trace-parameter effects	Transistor-based drivers and receivers for ALS and FAST technologies, Spice compatible	Simulates effects of board parameters and backplane interfaces; interfaces include Intergraph, Mentor Graphics, Valid Logic, Racal-Redac
Sun OS, Aegis/Domain OS, HP-UX, CLIX, Ultrix	Boundary-element field solver automatically determines trace electromagnetic coupling; cross-section comparison	Results reported as component, pin listing, net lengths, worst-case cross talk, etc.	Behavioral drivers and receivers; models for CMOS, BiCMOS, ECL, TTL	Full screening tool that determines critical nets for cross-talk transmission-line problems; automatic determination of critical nets; layout interfaces
Unix, Aegis/Domain OS	Boundary-element analysis to determine electromagnetic coupling	Tables and graphics; interactive operation lets user track and display signal distortion	Model libraries for CMOS, TTL, ECL, AC	Interacts with Mentor's Board Station; prerouting analysis; back annotation to critical-path analyzer
Unix, Aegis/Domain OS	Board cross-talk analyzer performs full electrical analyses of components, track, and board characteristics (propagation delays, track impedance, terminations in conjunction with parallel and adjacent routing)	Cross-talk analysis on high-speed boards employing user-customized technology rules	—	All design data automatically extracted from layout
Unix, VMS, Ultrix, AIX	Interactive or batch analysis of mixed-technology boards, MCMs, hybrids	Reflection, crosstalk, thermal noise, ohmic loss	7000 components	See footnote 2

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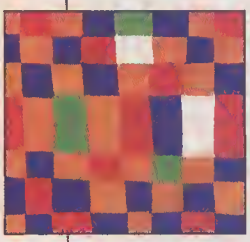
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Circle No. 222

Spectrum staff—Board tools proliferate

Displaying processed data

Through the use of data acquisition software, engineers are able to capture, analyze, view, and assimilate more data on product performance—no wonder these tools are booming



The more profoundly scientists and engineers investigate natural phenomena, the greater their dependence on data acquisition equipment. The greater the emphasis on process and quality control, the more urgent the need for data collection and manipulation tools. In short, data acquisition has become a big business.

As that business has spread, so have the diversity and breadth of commensurate hardware and software. Engineers no longer must develop their own equipment or write their own software. An array of commercial hardware provides every conceivable function—from preconditioning and analog-to-digital conversion, to encoding, signal processing, and returning to the analog world. With the rise of personal computers, much of the hardware takes the form of plug-in boards for the venerable IBM PC family or the Apple Macintosh. An equally dazzling array of commercial software running on those machines stands ready to help.

Many available software packages not only control the myriad of analog and digital input-output (I/O) boards, but also process, analyze, and display the incoming data in almost any conceivable form. Other packages specialize in just the analysis or display segment, or both, leaving the capturing process to sister software.

Data acquisition software has come far. In the process, much of the emphasis has been on isolating engineers from the tedious, line-by-line programming effort traditionally needed to produce application software. Contemporary commercial software has performed much of that work, putting the results into objects icons that an engineer simply interconnects on-screen, using a mouse or a keyboard. Other software offers menus for building application programs or provides high-level language bases, like C, from which to construct the desired program.

Included within the objects or menus are software drivers for hundreds of instruments and I/O boards, both analog and digital. Thus engineers need not learn the particular programming commands for all the possible hardware elements within a given measuring system. In some cases, looking at the computer screen is about the same as looking at the front panels (if there are any) of the equipment; changing functions and ranges on-screen is about the same as doing it *in situ* on the actual hardware. This approach to controlling instru-

Spectrum *staff*

1. Representative packages for data capture and control

Package	Company	Year first available	Price, US $	Platforms	Operating system
Global Lab Bases Package	Data Translation Inc.	1990	$995 (optional FFT module: $595)	IBM PC/XT/AT, PS/2	DOS
Hypersignal Workstation	Hyperception Inc.	1987 (updated 1990)	$989	IBM PC/XT/AT/386, PS/2, and compatibles	DOS
Asyst 3.1	Keithley Asyst	1985 (updated 1990)	$2145–$2995	IBM PC/XT/AT/386, PS/2, and compatibles	DOS
LabTech Notebook	Laboratory Technologies	1984 (updated 1990)	$995–$2000	IBM PC family, Mac II, DEC, Sun, HP/Apollo, IBM, ModComp, Concurrent, Tektronix, Texas Microsystems, Interactive Systems, Venturco	DOS, DS/2, MAC OS, Unix
LabView 2.0	National Instruments	1986 (updated 1990)	$1995	Macintosh family	MAC OS
LabOBJX	Scientific Software Tools Inc.	1990	$1995	PC AT/386/486	OOS (Windows 3.0 required)
N! Power	Signal Technology Inc.	1990	$1000–$15 000	OEC (VAX, RISC); Sun 3, 4	VMS, Ultrix, Unix
Speech Workstation	Spectrum Signal Processing Inc.	1990	$5995	IBM PC/AT/386	OOS
Workbench-Mac/PC	Strawberry Tree Inc.	1990	$995	IBM and Mac families	DOS, MAC OS

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ments, however, has its drawbacks. It is limited to one instrument at a time, and maximum speeds may not be achieved. Those needing maximum throughput may elect to program "at the command line," using C or some other high-level language, or even in an assembly language.

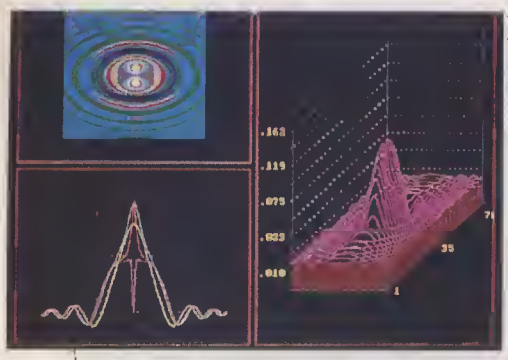
The acquisition packages shown in the following tables outline some of those capabilities. The listings are not comprehensive; they are meant to be only a representative sprinkling of the hundreds of commercial packages available today. The table is broken into three categories: front-end software for data capture and control, which may or may not include analysis and display features; software that specializes in analysis and display, accepting files from front-end software or other computer programs such as spreadsheets; and software that excels in displaying results in every conceivable fashion.

Many of the packages work on the fly, analyzing and displaying information as it comes in. Others store the information in RAM or on a disk, performing a post-analysis later. Some do both. Differences in analytical functions appear to depend on the variety and depth of data manipulation. Most commercial software begins analysis with a fast Fourier transform (FFT). After that, it is a question of the kind of statistical, numerical, filtering, or other function brought to bear. Some applications, like speech or audio processing, call for their own analysis and display methods, perhaps relying on digital signal processing.

Display capabilities are as varied as those for analysis. However, as software begins to specialize, it also begins to expand its math and display prowess.

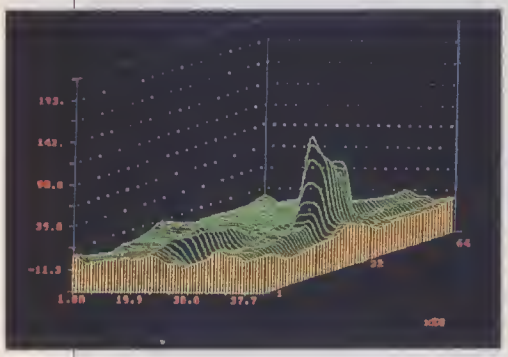
As for performance, that depends a great deal upon hardware configuration as well as on a software package's time-critical elements. Hardware includes not just the I/O boards or instruments under control, but also the architecture of the host computer. Thus actual data rates can be a function of disk throughput, for example, or RAM speed, or bus speed. Speed

Data rates	Acquisition method and interface	Analysis functions	Display functions	Export file formats	Comments
250-kHz throughput to and from disk	Menu-driven control of A/D board, counter-timer functions	Statistics, FFT, inverse FFT, auto/cross spectrum, windowing, transfer functions, filters, arithmetic operations, signal editing, curve fitting and interpolation, trig functions	Displays data as acquired	ASCII, binary, spreadsheets; also signed or unsigned word, byte, or long formats; 16-bit floating-point or 32-bit real formats	Gap-free hard-disk data transfer at maximum board throughput
1 MHz	Menu-driven, user-defined modules support DSP and other board functions; various hardware boards supported	FFT, FIR, and IIR filters; difference equations; signal editing; arithmetic, calculus, and trig functions; windowing, transfer function	Time and frequency domain, 2-D and 3-D spectrographs, arbitrary filter editor, unwrapped phase, pole-zero	ASCII, binary	Digital signal processing for DSP development and real-time continuous (gap-free) acquisition to disk
Hardware restricted	Programmable control of I/O, A/D, D/A boards, IEEE 488, and RS-232	FFTs, smoothing, convolutions, windows, calculus, curve fitting, statistics, histograms, matrices, filtering, peak detection, trig functions	Real-time display, x-y, contour, pie, bar, log linear, polar, axonometric, user windows, symbol, line types, labels, user-customizable	ASCII, binary, Lotus 1-2-3, PCX, HPGL, Asyst Data File format	Users assemble system from four modules; other software packages: Asystant GPIB controls IEEE 488 instruments with menu-driven analysis and graphics
Hardware restricted	Menu-driven control or ICONview graphical overlay controls, instruments, modules, and boards	Real-time analysis, curve fitting, FFT post-analysis	*t* vs. *y*, *x* vs. *y*, vertical and horizontal bars, digital meters	ASCII, binary, spreadsheet	Real-time process control and display
1 Msample/s	Icons control IEEE 488, RS-232, and VXI instruments and plug-in A/D, D/A and I/O boards	Real-time analysis, statistics, DSP filters, numerical analysis	Linear, log, bar, histograms, multiplot scatter plots, stripcharts, user-customizable	ASCII, binary, spreadsheet	Software modules represent virtual instruments with front-panel interface and block-diagram graphical programming
Hardware restricted	Menu-driven and programmable, compiled object-oriented graphical language controls A/D, I/O, RS-232 and IEEE 488 instruments, and DSP hardware	FFT, linear and nonlinear curve fitting, Kurtosis, Gaussian, Chi-square, filtering, matrices, arithmetic functions, histograms, other statistics	Linear, log, polar, 3-D axonometric, mesh, bars, histograms, pie charts, windows, viewports	ASCII, binary, Lotus 1-2-3	Supports popular data-acquisition hardware
Hardware restricted	Menu or command control, multichannel, A/D, D/A, IEEE 488	Complex math, speech, spectral analysis, digital filtering, matrix decision support	Real-time, 2-D and 3-D image, X-windows, Motif	ASCII, binary, ILS, user-defined	Object-oriented, Lisp commands, menus, run-time-add user routines
40 kHz/channel	Menu-driven capture of two-channel audio signals	FFT, linear predictive coding	Multiwindow spectrographs, slices, frequency contours, time waveforms, energy calculations	ASCII, binary, output to laser, inkjet printers	Audio-signal–processing analysis package
Hardware restricted	Mouse-driven icons configure A/D, I/O boards and instruments	Statistics, trig functions, calculus, scaling	Statistics, trig, arithmetic, calculus, scaling	ASCII	Intuitive environment interconnects icons to program and measure



Photos by Kelthley Asyst

Some data acquisition software packages are really high-level programming languages that integrate acquisition, control, analysis, and display. Thus the acquired signal can be displayed in complex forms.



A contour plot would be difficult to generate if the user had to describe how raw data had to be handled for display. The above plot, however, was created with a single command: AXON.PLOT.

of analysis is another matter. Rarely mentioned on data sheets, analysis speed also depends upon a number of factors, such as the kinds of algorithms used, whether a math coprocessor is supported, and how many data points are included.

Many packages used in data acquisition are intended for specialized applications and therefore are not listed.

Finally, there are dozens of commercial mathematics and graphics, and plotting programs that can find application in acquisition. For example, one menu-driven symbolic math system—Derive, from Soft Warehouse in Honolulu, Hawaii—literally puts the bulk of mathematical knowledge—from arithmetic to vectors to differential equations—on a floppy disk. Two other popular math packages are Mathematica from Wolfram Research Inc. in Champaign, Ill., and MathCAD from MathSoftInc., Cambridge, Mass. The Macintosh, with its generic propensity for displaying artwork, continues to attract a bevy of plotting tools. Among the newest are CA-Cricket Graph from Computer Associates International Inc., Malvern, Pa.; KaleidaGraph from Synergy Software, Reading, Pa.; and Delta Graph from DeltaPoint Inc., Monterey, Calif. ◆

2. Representative packages for data analysis and display

Package	Company	Year first available	Price, US $	Platform	Operating system
Tech *Graph* Pad	Binary Engineering	1987	$395	IBM PC and compatibles	DOS
Tekcalc	BV Engineering	1986	$150	IBM PC family	DOS
DSPlay XL	Burr-Brown Corp.	1988 (updated 1990)	$1495	IBM PC and compatibles	DOS
Dadisp	DSP Development Corp.	1986 (updated 1989)	$895–$6995	IBM PC, PS/2; HP, Sun, DEC, IBM workstations	DOS
Hypersignal-Plus	Hyperception Inc.	1985	$489	IBM PC/XT/AT/386 and compatibles	DOS
SigmaPlot	Jandel Scientific	1985 (updated regularly)	$495	IBM PC/XT/AT, PS/2 and compatibles	DOS
Matlab	The Mathworks Inc.	1985	$695(PC), $795(Mac)	PC/386, Mac, Sun, HP, HP/Apollo, VAX, DECstation, others	DOS, Mac OS, VMS, Unix, Domain, others
TempleGraph Academic/Government	Mihalisin Associates	1987	$990–$1290	Sun, Solbourne	Unix, Sun OS
Interactive Laboratory System (ILS)	Signal Technology Inc.	1979 (updated regularly)	$1000–$15 000	DEC, Sun, Apollo, HP, Concurrent, PC	DOS, VMS, Ultrix, Unix
Speakeasy	Speakeasy Computing Corp.	1965 (updated regularly)	$2000–$5000/year	IBM 6000, RT, PS/2; Sun 3, 4; DECstation	AIX, Sun OS, VMS, Ultrix
EasyPlot Academic/Government	Spiral Software	1988	$269–$349	IBM PC/XT/AT, PS/2, and compatibles	DOS
CSS/3:Statistica	StatSoft Inc.	1990	$795	IBM PC/XT/AT, PS/2, and compatibles	DOS
Graftool, 3.0	3-D Visions Inc	—	$495	IBM PC/XT/AT, PS/2, and compatibles	DOS
Axum Academic/Government	TriMetrix Inc.	1989	$495	IBM PC/XT/AT, PS/2, and compatibles	DOS

3. Representative packages specializing in display

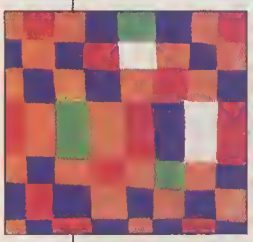
Package	Company	Year first available	Price, US $	Platform	Operating system
GrafMaker	BV Engineering	1990	$195	IBM PC family	DOS
NDP Plot	MicroWay Inc.	1988	$325	PC 386/486 with Intel or Weitek coprocessor	DOS
TempleGo	Mihalisin Associates	1989	$495	Sun, Solbourne	Unix, Sun OS

Analysis capabilities	Display capabilities	Graphics compatibility	Import/export file formats	Comments
Curve fitting, data-smoothing, probability analysis, and more	Linear, log/log, linear/log, probability, histogram, and polar plots; error bars, descending scales, multiple axes, symbols, labels	CGA, EGA, VGA, Hercules	Imports: ASCII, binary, Lotus and Symphony spreadsheet files, (.WKS, .WK1, .WR1) Exports: PostScript, HPGL, .PIC	Built-in "spreadsheet browse mode"; with Auto*TGP, directly integrates T*G*P graphics capabilities into user's application
Statistics, curve fitting, standard deviation, linear regression	Parametric graphing of user-entered functions, line graphs of functions of disk-data	CGA	ASCII, 512 points maximum	None
Any DSP algorithm definable from 100+ function library, including FFT, FIR, IIR; custom functions	*x-y*, polar, waterfall, spectrographs, landscape	EGA, VGA	ASCII, binary	Works with DSP board; code generated can be executed in any DSP32/32C application
Over 200 processing functions: FFT, complex math, peaks, signal editing, calculus, others	*x-y*, tabular, waterfall, graphical series in overlapping or tiled windows	CGA, EGA, VGA, Hercules	ASCII, binary, Lotus PRN	Windowed, menu-driven spreadsheet, user-customizable macro facility
FFT, FIR, and IIR filters; difference equations, complete statistical processing	Time and frequency domain, 2-D and 3-D spectrographs	CGA, EGA, VGA, Hercules, SuperVGA	ASCII, binary	Subset of Hypersignal workstation
Descriptive statistics, t-tests, error bars, data manipulation, transforms, curve fitting (nonlinear, linear, and others)	Scatter and box plots, line, bar, stacked bar, histograms, pie charts, quality-control graphs	CGA, EGA, VGA, Hercules	Imports: DIF, ASCII, Lotus (.WKS, .WK1) Exports: ASCII, DIF, HPGL, SCODL, LL, PostScript, Metafiles	Math symbols, Greek letters, superscripts, subscripts, grid
Matrix computation, signal processing, filtering, FFTs, equation solving, statistics, curve fitting, application Toolboxes	2-D linear, log, bar, log-log, semilog, polar, 3-D mesh, contour	CGA, EGA, VGA, Hercules, X-windows, SunView graphics terminals	Imports: ASCII Exports: HPGL, PostScript	Interactive and programmable
Statistics, calculus, curve fitting, vector math, smoothing, transformations	Line/scatter plots, bars with error bar, spline, legend and log axes, text charts	Sun, Solbourne monitors	Imports: ASCII Exports: PostScript	Math symbols: integrals, partial derivatives, gradient, divergence, Greek letters
Spectral analysis, statistics, digital filtering, speech processing, pattern analysis	Scatter plots, bars, bit-mapping, half-tone, 2-D and 3-D displays, windows, overlapped displays	EGA, VGA, SunView, Apollo, GMR, DEC WS/Regis, Color	ASCII, binary	PostScript, ASCII, symbol set, customizable menus
Full numerical and statistical analysis, linear and quadratic programming, differential equations	Bit maps, pie and bar charts, tower charts, contour, 2-D and 3-D graphics	Tektronix, DEC WS/Regis, X-windows, SunView	Imports/exports: ASCII, Fortran Exports: HPLaserjet, HPGL, Postscript	User-extendable, interactive and programmable
Statistics, nonlinear curve fitting, cubic spline, FFT, calculus, smoothing	Linear, semilog, log-log, polar, contours, 3-D, *x-y*	EGA, VGA, Hercules	Imports: ASCII, spreadsheet Exports: PostScript, HP Laserjet and DeskJet, dot matrix	Greek and math symbols, superscripts, subscripts; unlimited points, curves, graphs, pages
Fourier decomposition, full statistics	Lines, bars, step, area, box, scatter, 3-D, contour, surface plots, others	EGA, VGA, AT&T, Hercules 8514/A	Imports/ exports: ASCII, Lotus, Excel, DIF, SYLK; Exports: HPGL, CGM, PostScript	Supports all IBM extended graphics characters
On-screen formula-solver, statistics, curve fitting, 2-D and 3-D contouring, FFT, others	2-D and 3-D scatter plots, polar plots, multiple axes, log and probability, 3-D surfaces, others	CGA, EGA, VGA, Hercules	Imports: ASCII, Lotus, Excel, others Exports: Lotus, Word, others	Mouse support, 256 million points, intelligent data cursor, spreadsheet, color contours
Statistics, Anova, correlation, regression, curve fitting, data smoothing	2-D and 3-D line, 3-D mesh, spline, scatter, 2-D and 3-D bar, pie, polar, Smith charts, others	CGA, EGA, VGA, Hercules, others	Imports: ASCII, Lotus, dBase Exports: Lotus, .PIC, HPGL, GEM, PostScript, Tektronix	Supports 21 fonts, super- and subscripts, interactive graph, and 100 functions

Analysis capabilities	Display capabilities	Graphics compatibility	Import/export file formats	Comments
Integral, differential, math operations on data files, + − * / or exponentiate by constant, + − * / by a file	Bar, stacked bar, stock and polar charts, error bars, line graphs, two *x* and two *y* axes independently linear or log	CGA, EGA, VGA, Hercules	Imports: ASCII Exports: HPGL, DM/PL, SPGL, RDGL, and more	Over 30 plotters supported; printer output to Epson dot matrix or Laserjet printers
Curve fitting (producing an axis line or a smooth curved line through a series of scaled or unscaled data points)	3-D graphics functions for contouring, elevation plotting with hidden-line removal, 3-D object viewing and rotation; can generate 2-D or 3-D plots; source-code compatible with mainframe Celcomp calls	CGA, EGA, VGA, and monochrome plotters and printers	–	None.
N.A.	Line/scatter plots, bars with error bar, spline, legend and log axes, text charts	Sun, Solbourne monitors	Imports: ASCII Exports: PostScript	Math symbols: integrals, partial derivative, derivative, gradient, devergences, Greek letters

User-friendly CAE

To make it easier for engineers and managers to productively use CAE tools, industry is trying to devise a common framework of interface and management software



Within the last two years, users and developers of computer-aided engineering (CAE) software have begun to explore ways of using it better. The packages discussed in the preceding sections of this guide automate a wide range of engineering tasks. However, it is often difficult for engineers who are used to one brand of tool to become accustomed to a different tool. For managers, keeping track of the status of a project—how much has been completed, who worked on what version of a design, which released version of a tool was used, and so forth—can be a monumental task.

For example, suppose a designer creates a schematic of a board and then wants to run a simulation. He or she will work more efficiently if that simulator's interface resembles that of familiar tools. For instance, it should be possible to activate the tool in the same way as other tools, tool functions should appear in the same place on the screen as for other tools, and similar functions (such as delete) should be called into action in the same way.

Once the simulation is successful, the design would pass to another engineer who would use different software to lay out the board with real components. Ideally, the two engineers should be able to swap information back and forth in electronic form, the layout engineer using the designer's information as direct input to the layout software and passing the laid-out design back to the designer to double-check its operation by re-simulating it.

In reality, though, this is often difficult. The same tools may have slightly different interfaces in versions for different operating systems and different computers, and similar tools may implement the same function in different ways. The data formats used by two engineers may differ and so require translation. The data required to perform one task may be missing from the data required by another and need to be added manually. The two software packages may keep track of data differently, so that two databases have to be maintained and updated uniformly. When multiple software packages and engineers are involved, logistical nightmares are likely and can slow down development drastically.

Spectrum *Staff*

Levels of standards

The more CAE packages there are, the more users experience these problems, and the CAE industry is developing practical ways of solving them. For instance, to express such information as package dimensions and pin callouts in a standard fashion, EDIF was created [p.68]. And so that engineers may describe functional aspects of a system in the same way, high-level hardware-description languages such as VHDL and Verilog HDL have been developed.

Now, to provide a consistent interface and to help manage and control the flow of data, they are taking an approach called an open framework. An open framework is to CAE software what a standard backplane is to hardware; it specifies how data will get from one point to another. More concretely, a framework is a set of specifications that describe how users will locate and use a CAE software package, and what tools will be a standard part of an easy-to-manage environment. Some see it, in fact, as an environment that is layered on top of a general-purpose operating system, such as Unix.

Two years ago, users and suppliers formed the Computer Framework Initiative consortium to create standards so that software packages from different vendors work together; last June at the Design Automation Conference in Orlando, Fla., the consortium demonstrated a prototype environment in which different software packages shared information. In the consortium's language, a "producer" package generated information that is passed to a "consumer" package, which can use the information directly to perform its tasks.

These packages are able to transfer information because they have been adapted to work with the CFI procedural interface (PI). The producer and consumer tools are able to write and read (respectively) netlists in the format defined by the PI and so the interface is able to move information between them.

CFI's PI was developed in eight months by its Design Representation Technical Subcommittee and tested a month before it was shown for the first time in June. The demonstration used software running on platforms from Hewlett-Packard, Digital Equipment, IBM, and Sun Microsystems, thus demonstrating the framework's hardware independence.

Among the software suppliers participating in the demonstration were AT&T Bell Laboratories, Cadence Design Systems, Computervision, DataXpress, GenRad, Hewlett-Packard, IBM, Microelectronics and Computer Technology Corp. (MCC), Mentor Graphics, NCR Microelectronics, Objectivity, Ontologic, Racal-Redac, Siemens, University of California—Berkeley, Valid Logic, Viewlogic Systems, VLSI Technology, and Zycad. With this range of participation, it is likely that the standard will have a great deal of support when it is released.

Formal publication of the PI guideline is scheduled to take place this month. But standardization work will continue, as other CFI subcommittees work on design data management, design methodology, intertool communication, design representation, systems environments, and the overall framework architecture. These subcommittees are also working with other standards organizations, among them the IEEE and the International Standards Organization (ISO), to influence the direction of work already under way.

At the same time, suppliers are beginning to work together to create their own frameworks and make them commercially available. In the following tables, three recent commercial examples are listed: the Falcon Framework created by Mentor Graphics Inc. of Beaverton, Ore. [Table 1]; PowerFrame, a joint venture of Digital Equipment Corp. of Maynard, Mass., and Cadence Design Systems of Lowell, Mass. [Table 2]; and Design Framework II developed by Cadence alone [Table 3]. The tables present a sampling of software tools from vendors who are not the major sponsors. (It should be understood that the framework sponsors themselves supply tools that work within the framework.) Further, many of the vendors listed supply more than one tool that works under the framework; space limitations prevent listing all the tools.

Under its "Open Door" program, Mentor invited other suppliers of CAE tools to work with it to make their products compatible with Mentor's Falcon Frame-

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work. This framework was originally created by Mentor so that its own tools would work together; now the company is sharing its data formats and requirements (called EDDF for Engineering Design Data Format) with other vendors, so that they can link in. Because data formats are specified, the software packages become closely coupled. This framework currently covers applications that run on HP/Apollo and Sun Microsystems workstations that are supported by Mentor.

The Digital/Cadence PowerFrame differs from Falcon in that it is a loosely coupled set of tools. The two companies were founding members of the Computer Framework Initiative and have been working closely with the group to ensure that their framework will be compatible with its specifications, once they are formalized. Rather than change tools to meet new requirements, existing tools are "encapsulated" in a software shell that lets them communicate with other tools.

PowerFrame, which is referred to as a management framework, allows different workstations and computers into a CAE network and obviates the need to move applications to a particular workstation. Digital will work with companies that use HP/Apollo or Sun, as well as Digital, workstations to encapsulate existing tools for PowerFrame. The framework provides a common way of accessing the tools and a way of controlling which versions of the tools and of the design data are used by different groups. Digital will customize the framework to a company's needs.

Design Framework II from Cadence, as the name implies, concentrates on integrating design tools. A major advocate of frameworks, Cadence has already been through its first version of an open framework. It will continue to support Design Framework II to let design tools work well together, in addition to supporting PowerFrame so that its customers can manage the entire engineering process.

◆

1. Representative sample of CAE packages for Falcon Framework (Mentor Graphics)

Package	Company	Year first available	Price, US $	Function	Description
Saber	Analogy Inc.	1987	$15 000	Analog, mixed-mode simulation	Able to simulate mixed-level (i.e., IC, board, system-level) designs; has native mixed-signal capability as well as interfaces to Cadat and Verilog digital simulators; modeling capabilities
Relink	Eckert Enterprises	1989	$1500	Database maintenance	Restructures, recovers, or archives Mentor databases; works with distributed database; allows switching from shared to separate libraries; compatible with Mentor's layout, schematic, and documentation tools
Academy	EEsof Inc.	1990	$14 000	Framework for analog circuit and system simulation	Work environment for design entry, simulation (including analysis, optimization, and tuning), mask layout, and documentation
HSpice HSPlot	Meta-Software Inc.	1976	$4000–$90 000	Analog simulation	Spice-derivative simulator able to model high-performance CMOS, BiCMOS, ECL, and GaAs; supports submicrometer MOS, poly-emitter BJT, enhancement/depletion GaAs
CapFast CF3000M	Phase Three Logic Inc.	1986 (upgraded 1990)	Contact vendor	Schematic capture	Translates Mentor symbol libraries for use on a PC, resultant schematics back to Mentor format; provides full schematic translation compatible with EDIF 2.0.0
TLC	Quad Design Technology Inc.	—	—	Transmission-line analysis	Advanced digital system simulation calculates and displays effects of transmission-line phenomena; predicts ringing, non-incident switching, undershoot, overshoot, and time delay for networks of arbitrary topology and construction
BoardScan	Quantic Laboratories Inc.	1990	—	Board layout analysis	Determines critical nets on boards where cross talk and other transmission-line problems are likely to occur; optional interface to Greenfield
ChipCrafter family	Seattle Silicon	1988	$59 000–$149 000	Tool kits for ASIC and IC design	Integrated tool set for developing complex ICs and ASICs that can be targeted to any CMOS process; advanced users can fine-tune designs and import custom cells or cores
Mixim	Swiftlogic Ltd.	1989	$15 000	Mixed-signal simulation	An extension of Mentor's QuicSim for mixed-signal designs in QuicSim environment; event-driven, so uses voltage steps rather than mixed-signal time steps
VHDL Compiler	Synopsis Inc.	—	—	Logic synthesis	Synthesizes RTL design descriptions in IEEE VHDL for optimization by the Design Compiler and ECL Compiler (also available in framework versions)
TDS	TSSI	1986	$19 000+	Tool kit for test development	Uses simulation data to perform design behavior analysis, specification verification, tester resource optimization, and test program generation; supports over 30 simulators and over 80 models of ATE
Vantage Spreadsheet	Vantage Analysis Systems Inc.	1989	$44 000	VHDL simulation	Works from schematic or VHDL source description, which can be modified during simulation without stopping or resetting; accepts and produces schematics in Mentor, Valid, or EDIF 2.0.0 format

2. Representative sample of CAE packages for PowerFrame framework (Digital Equipment Corp./Cadence Design Systems)

Package	Company	Year first available	Price, US $	Function	Description
Saber	Analogy Inc.	1987	$15 000	Analog, mixed-mode simulation	Can simulate mixed-level (i.e., IC, board, system level) designs; has native mixed-signal capability as well as interfaces to Cadat and Verilog digital simulators' modeling capabilities
Verilog-XL	Cadence Design Systems Inc.	—	—	Digital logic simulation	Supports top-down and mixed-level design techniques; integral hardware description language (HDL) covers input stimulus, output formatting, simulation control, debugging control
Abel-4PLD	Data I/O Corp.	1984	$1995	Programmable-IC (PIC) design	Implements logic designs targeted for over 6000 PIC types; designs are entered behaviorally, and can automatically be simulated, synthesized, and converted into industry-standard output formats; includes Jedec, PLDs, ABEL-PLA files for FPGAs/gate arrays, and PROM translation files for PROMs
System HILO	Genrad Inc.	1988	$10 500+	Digital simulation	Integrated set of design analysis, verification, and test generation modules for optimizing ASIC and board designs and test programs
Scicards	Harris/Scientific Calculations Inc.	1978	—	Board layout and routing	Integrated CAD system for circuit board and hybrid circuit design; offers gridded, gridless, flood, and specialized routers, on-line design-rule checking, and advanced SMT, hybrid, and high-speed logic capabilities
Viewdraw	Viewlogic (encapsulated for framework by Harris/Scientific Calculations Inc.)	—	—	Schematic capture	Speeds creation of symbols, schematics, block diagrams, generic graphics; libraries hold over 4000 symbols and parts for ASIC, analog, microwave design
HSpice	Meta-Software Inc.	1976	$4000–$90 000	Analog simulation	Spice-derivative, able to model high-performance CMOS, BiCMOS, ECL, and GaAs; supports submicrometer MOS, poly-emitter BJT, and enhancement/depletion GaAs
SL-Design	Silvar-Lisco	1990	$15 000	Schematic entry	Permits top-down design; on-line features include symbol generation, netlist error checking, macro creation; full read/write access to database
HDL Compiler	Synopsis Inc.	—	—	Logic synthesis	Synthesizes RTL design descriptions for optimization on Design Compiler and ECL Compiler (also available in framework versions)
Lasar V6	Teradyne Inc.	—	$20 000	Simulation	Multilevel logic and fault simulation with test generation capability
Allegro	Valid Logic Systems	—	—	Layout placement, routing	Board design system driven by engineering-specified rules; expert routing system and tools for high-speed designs, thermal analysis, testability and manufacturability

3. Representative sample of CAE packages for Design Framework II (Cadence Design Systems)

Package	Company	Year first available	Price, US $	Function	Description
Microwave Harmonica	Compact Software	1990	$28 750–$34 500 per seat	Analog simulation	Simulates microwave and RF linear and nonlinear circuits
N.2	Data I/O Corp.	—	—	Digital simulation	Performs multilevel simulation of complete digital systems
Libra	EEsof Inc.	1988	$24 000	Analog simulation	Simulates microwave and RF linear and nonlinear circuits
EPIC	EPIC	—	—	Timing analysis	—
LSIM	Mentor Graphics Corp.	1990	—	Logic simulation	—
Analog Artist HSpice Interface	Meta-Software Inc.	1989	$5000	Analog design	Acts as interface to HSpice netlist, simulation control, waveform control, waveform display, and other analog functions
em	Sonnet Software	1989	$30 000	Electromagnetic analysis	Evaluates predominantly planar circuits for all electromagnetic effects (method of moments) for the design of microwave and other high-performance digital applications

DSP software

(Continued from p. 59)

engineering software is sold in much smaller volume, vendors often lack the resources to meet that ideal.

Documentation for DSP software comes in assorted flavors. Monarch delivers a comprehensive manual, complete with background theory and references for each filter or operation in the package. Interestingly, most references were to the book, *Digital Filter Design Handbook*, by Fred Taylor, Momentum Data Systems' president. The Atlantic Signal manual looks photocopied rather than printed, a disappointing attribute for a US $1500 product. The demo copies of the other packages I received did not include the user's manual and support documents.

Software support is seldom a problem. Most vendors of DSP software are quite happy to talk to users, and will even help them with technical problems beyond those with which their software packages are concerned. Since DSP software packages are sold in relatively low volume, getting through on the phone is rarely a problem.

Software upgrade policies for engineering packages can come as an unpleasant surprise to first-time users. Few upgrade costs for DSP software are as generous as for the larger software packages. Again, the much smaller market requires that prices remain high to cover development costs.

User groups can be a big help, especially those that maintain a modem-accessible bulletin board.

About the author

Bruce C. Mather (M) is the acting manager of the machine perception section in the robotics and automation department, Automation and Data Systems Division, at the Southwest Research Institute in San Antonio, Texas. A specialist in digital signal processing and computer vision, he is currently managing a research project on the application of neural networks to shape recognition. He also works in the areas of biomedical instrumentation, high-speed image processing, and robotics. He received his electrical engineering degrees from the University of Illinois at Champaign-Urbana. ◆

EM simulators

(Continued from p. 77)

as the preconditioned conjugate gradient algorithm) used in the software, or does the solution time grow rapidly with increasing problem size, thus limiting its usefulness in the design of complex, high-speed circuits?

Postprocessing

- Interactive interface. Is the user interface fully interactive with pop-up menus and graphics oriented commands to simplify the operation of the program?
- Plotting. Are contour and shaded images of scalar fields, vector plots of vector fields, and magnitude versus distance graphs available?
- Direct display. Are such common quantities as capacitance, energy, and force easily displayed by direct menu commands? Can you add user-defined quantities to the menu for direct display?
- Calculator. Does the software include a calculator to combine and to manipulate scalar and vector fields in one, two, and three dimensions?
- Macro. Does the software support a macro capability to automate repetitive calculations?
- Output compatibility. Can all derived quantities be output in standard data formats, including those used by common circuit simulation programs?

About the author

Zoltan J. Cendes (M) is cofounder of Ansoft Corp., Pittsburgh, a company specializing in finite-element electromagnetic software, and a professor of electrical and computer engineering at Carnegie Mellon University, Pittsburgh. He previously developed finite-element computer-aided engineering systems at General Electric Co. He has a bachelor's degree in engineering science from the University of Michigan in Ann Arbor and a master's and doctorate in electrical engineering from McGill University, Montreal. ◆

Analog design

(Continued from p. 67)

with up to 200 transistors. A change was made in the look-up tables for the Macintosh version and in the 286- and 386-specific versions of IsSpice, however, so the program can use additional memory that these machines address to simulate larger circuits. The maximum circuit size for these versions can again be estimated by Blume's 250-transistors-per-megabyte-of-RAM rule.

Since the 386-protected mode is about 30 percent faster than 8088 real mode, there is a marked speed advantage to 386 users who run 386-protected-mode IsSpice instead of the 8088-real-mode or the 286-protected-mode IsSpice. However, neither the 286- nor 386-protected-mode IsSpice allows multitasking. This is a good, usable, but limited product at a reasonable price.

Graphics postprocessors

Graphics postprocessors [Table 3] create screen displays of data calculated by Spice. A good postprocessor will be able to access all the data generated by Spice, not just the data saved in the Spice output file. Also, it will mathematically manipulate the data to clarify its meaning. There are only two postprocessors available for Spice on personal computers: MicroSim's Probe and Intusoft's IntuScope.

Probe displays and manipulates data from a special file created by PSpice during a simulation run. It is exceptionally easy to use, because it employs standard algebraic notation and fill-in-the-blanks menus. Further, unless the user specifically tells PSpice not to save voltages and currents at certain nodes, the voltages and currents from all nodes are available to Probe.

Probe's greatest strength—its use of PSpice's automatically created special output file—is also its greatest weakness. PSpice stores data in the output file in single-precision format, so calculations using two variables of approximately the same size, or a small variable, will not give totally accurate answers. Also, Probe does not generate high-quality graphics output for manuals and design documents. A user will need a program like Adobe's StreamLine, which converts low-resolution bitmap graphics into high-resolution vector graphics, to create presentation graphics from Probe.

With IntuScope, designers can display and mathematically manipulate data from Spice output files generated by any program that uses the Spice 2G6 output format. The postprocessor lets them use a PC or Mac to study the results of simulations run on other computers. IntuScope generates high-quality graphics (suitable for use in papers, reports, and presentations) and employs the full double-precision value of a number, things that Probe does not do, so it gives the designer a truer feel for circuit behavior when voltages and/or currents are close to zero.

The current version of IntuScope for IBM-compatible PCs uses a reverse-Polish-notation (RPN) interface that's difficult to deal with, even for designers familiar with HP's RPN calculators. However, the current Mac version of IntuSoft (and the next PC version) has a WIMP interface that is simpler to use. Also, IntuScope can only access data stored in the print tables of Spice output files; if data was not saved during the simulation to a .PRINT table, it is unavailable to IntuScope—a significant limitation.

About the author

John Richard Hines (M) is a silicon sensor engineer at Honeywell Optoelectronics, in Richardson, Texas, and a registered professional engineer. He holds three patents for circuit design techniques and has filed patents for techniques that can be used to fabricate integrated silicon sensors. Hines writes extensively about the use of personal computers in engineering for a variety of publications. ◆

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Digital signal processing

Digital Signal Analysis, written by Samuel D. Sterns and Don R. Rush (Prentice-Hall Inc., New York, 2nd ed., 1990) not only provides the reader with a thorough review of the fundamentals of digital signal analysis and filter design, but also offers some software. The book comes with an IBM-PC–compatible 5.25-inch disk that includes transforms and filter design software in portable modules written in Fortran 77; they can be used for both study purposes and actual designs.

In the area of speech, the International Conference on Spoken Language Processing–ICSLP will be held Nov. 18–22 in Kobe, Japan, at the International Conference Center Kobe. For further information, contact Hiroya Fujisaki, Department of Electronic Engineering, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113, Japan; (81+3) 812 4442, ext. 6656.

Digital signal processing is one of the many topics covered at the ACM/IEEE Design Automation Conference. The CAE industry's oldest and largest conference, this meeting marks its 28th anniversary next year, when it will be held June 16–20 in San Francisco. For information, write or call MP Associates Inc., 7490 Clubhouse Rd., Suite 102, Boulder, Colo. 80301; 303-530-4333. Past proceedings of this conference, available through the IEEE, are also an excellent source of information on DSP, analog design, and other topics covered in this special focus report.

Analog design

There are many good books about analog design software, among them *A Spice Tutorial, A Spice User's Guide*, and *Spice Modeling Notes* (Oholiab Technology, Richardson, Texas, 1988), all written by John R. Hines, the author of the article appearing in this software focus report. These works provide a solid introduction to Spice simulation as well as practical information about using Spice and creating Spice models.

Another recently published text is *Analogue IC Design: The Current-mode Approach* by C. Toumazou et al. (Peter Peregrinus Ltd., London, 1990). This work offers an insight into some of the problems unique to analog design and provides a solution methodology.

EDIF

The EDIF standard is available as "Electronic Design Interchange Format," version 2.0.0, 2nd edition, 1990, ANSI/EIA Standard 548, from the Electronic Industries Association, Standard Sales Department, 1722 Eye St., N.W., Washington, D.C. 20006; 202-457-4966. Also available from the EIA is "EDIF Connectivity," EDIF monograph series, Vol. 2, EIA/EDIF-2.

The EIA also offers "Introduction to EDIF," Vol. I, in its EDIF monograph series, and a guide titled "Using EDIF for Schematic Transfer."

Co-author John Eurich presents the basics in "A Tutorial Introduction to Electronic Design Interchange Format" in the proceedings of the 23rd ACM/IEEE Design Automation Conference, June 1986. Tutorial videotapes on EDIF are available from Engineering DataXpress, whose address appears in the index.

The 1991 10th International Conference on Computer Hardware Description Languages is scheduled to take place on April 22–26 in Marseilles, France. Contact the IEEE Computer Society, Conference Department, 1730 Massachusetts Ave., N.W., Washington, D.C. 20036; 202-371-1013; fax, 212-728-0884.

EM and finite-element analysis

Zoltan J. Cendes has previously written on the topic of finite-element analysis for *IEEE Spectrum*; in the April 1989 issue, p. 29, he authored the article, "Unlocking the magic of Maxwell's equations," which discusses the use of finite-element analysis for device-level design.

Numerical Computation of Electric and Magnetic Fields (Van Nostrand Reinhold, New York, 1987) is a good introduction to the use of finite-element analysis for electromagnetics, while a discussion of the practical aspects of using that analysis in magnetic design appears in *Computer-Aided Design in Magnetics* by D.A. Lowther and Peter P. Silvester (Springer-Verlag, New York, 1986).

The proceedings of the 1990 biennial IEEE Conference on Electromagnetic Field Computations, which was held in Toronto last month, will be published in an upcoming issue of the *IEEE Transactions on Magnetics*.

CASE

Computer-Aided Software Design: Build Quality Software with CASE is an introduction to the field written by Max Schindler (John Wiley & Sons, New York, 1990). By taking a casual approach to the topic, the author makes a complex topic easy and enjoyable reading.

Ada, the CASE environment developed by the Department of Defense, Ada Joint Program, is the subject of a quarterly

newsletter, the "Ada Information Clearinghouse (AdaIC) Newsletter" (IIT Research Institute, Lanham, Md.). It keeps readers abreast of the current status of Ada and provides answers to readers' questions, European developments, and more.

"CASE tools for Artificial Intelligence" is the topic of the Computer Society Conference on Tools for AI—TAI '90. The meeting is to be held Nov. 6–9 at the Hyatt in Washington, D.C. To attend, contact Nikolaos G. Bourbakis, George Mason University, Department of ECE, Fairfax, Va. 22030; 703-425-3930.

In December, Irvine, Calif., will host a major CASE-industry conference: the Fourth International Workshop on CASE–CASE '90. To be held Dec. 5–8 at the Irvine Hilton and Towers, the conference will cover all aspects of CASE, including management of software development and other high-level concerns. To attend, contact Ronald Norman at San Diego State University College of Administration, San Diego, Calif. 92182; 619-594-3734.

Board software

The fields of board CAD, data acquisition, and CAE frameworks are currently the center of attention of the CAE industry, so many rapid developments are occurring in them. Fortunately, there are many conferences sponsored by the IEEE on these topics. As mentioned previously, the ACM/IEEE Design Automation Conference and its past proceedings are an invaluable source of information.

On Nov. 12–15, the International Conference on Computer-Aided Design–ICCAD '90 will be held at the Santa Clara Convention Center in Santa Clara, Calif. For more information, contact ICCAD '90, IEEE Computer Society, 1730 Massachussetts Ave., N.W., Washington, D.C. 20036; 202-371-1013.

On the East Coast of the United States, the High-Tech PC and Workstation Applications Conference will be held on Nov. 14 at the Governor Morris Inn (Royce Hotel), Morristown, N.J. To find out about attending, contact Donald Hsu, Box 2093, Fort Lee N.J. 07024; 201-585-1226 or 914-359-7800.

Frameworks

The 1990 2nd International IFIP (International Federation for Information Processing) Workshop on Electronic Design Automation Frameworks will take place at the University of Virginia in Charlottesville on Nov. 26–28. Contact the IEEE Computer Society (see under EDIF in this section).

General

The 1990 Conference on Software Maintenance will take place Nov. 26–29, 1990 in San Diego. It is sponsored by the IEEE Computer Society, the Association for Computing Machinery, the National Institute of Standards and Technology, and others. Contact the IEEE Computer Society (see under EDIF in this section).

Acknowledgments

IEEE Spectrum called upon many experts in preparing this special focus report. We are especially indebted to the following individuals for their advice, although their identification with the report should not be construed as their endorsement of the material included in it.

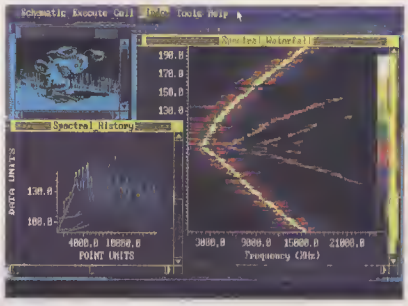
The advisors for this focus report were: Professor Ted G. Lewis, Computer Science Department, Bergen State University, Corvallis, Ore.; Dr. Robert Rutenbar, Electrical and Computer Engineering (ECE) Department, Carnegie Mellon University, Pittsburgh; Professor Guy Johnson, chairman, Department of Information Technology, Rochester Institute of Technology, Rochester, N.Y.; and Art J. de Geus, senior vice president, engineering, Synopsis Inc., Mountain View, Calif.

Also, Professor Don Thomas, ECE Department, Carnegie Mellon University, Pittsburgh, provided special help in reviewing the material on EDIF that appears here.

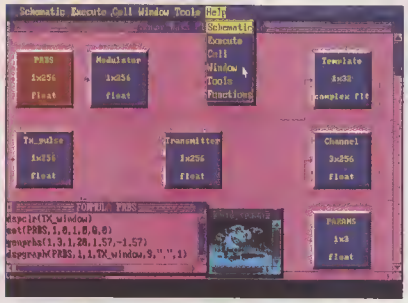
Spawn

A new concept in signal processing.

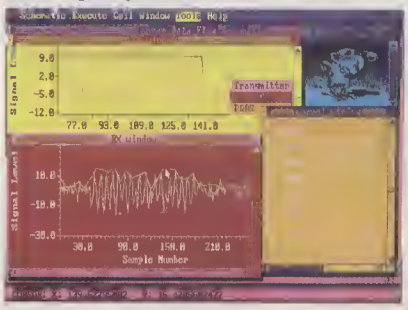
An affordable DSP environment for IBM PC/XT/AT compatibles capable of data analysis, signal processing and simulation, or custom real/post time application development in conjunction with external hardware. Object oriented processing, windows and an open architecture allow the engineer/scientist to focus on algorithms, interfaces and applications.



Object Oriented Framework
Data objects organized as scalars, vectors or matrices, include multi-line formulae, and depicted as cells on a processing schematic. Automatic schematic connections illustrate cell data flow or formula execution flow. A virtual cell structure provides arbitrary data capacity.



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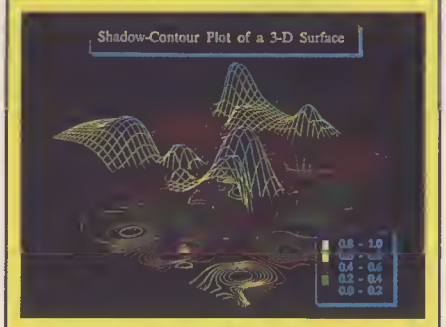
Open Architecture DSP Library
Extensive standard function library included for DSP and data analysis. Additional compiled functions can be linked into the run-time library. Application-specific libraries for hardware data acquisition, interface and control, and concurrent external signal processing.



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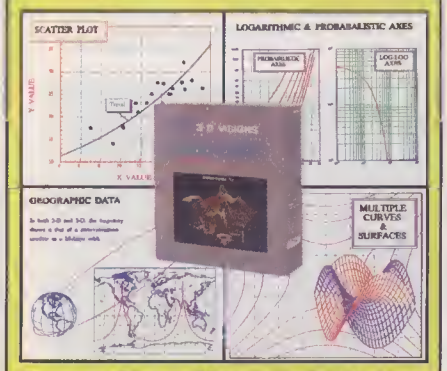
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INDEX

EDITORIAL

DIGITAL SIGNAL PROCESSING

Ariel Corp., 433 River Rd., Highland Park, NJ 08904, 201-249-2900 circle no. 251, p. 54
The Athena Group Inc., 3424 N.W. 31st St., Gainesville, FL 32605, 904-371-2567 circle no. 252, p. 54
Atlanta Signal Processors Inc., 770 Spring St., Atlanta, GA 30308, 404-892-7265 circle no. 253, p. 54
Burr-Brown Corp., 6550 South 8ay Colony Or., Suite 160, Tucson, AZ 85734, 602-746-1111 circle no. 254, p. 54
Comdisco Systems Inc., 919 E. Hillsdale 8lvd., Foster City, CA 94404, 415-574-5800 circle no. 255, **
DSP Development Corp., One Kendall Square, 8uilding 100, Cambridge, MA 02139, 617-577-1133 circle no. 256, p. 54
Dalanco Spry, 89 Westland Ave., Rochester, NY 1461B, 716-473-3610 circle no. 257, p. 54
DSP Research, 391 Balsam Ave., Sunnyvale, CA 94086, 408-773-1042 circle no. 25B, p. 54
Forth Inc., 111 N. Sepulveda Blvd., Suite 300, Manhattan 8each, CA 90266, 213-372-8493 circle no. 259, p. 54
Hyperception Inc., 9550 Skillman, Suite 302, 0allas, TX 75243, 214-343-8525 circle no. 260, p. 54
Intermetrics Inc., 733 Concord Ave., Cambridge, MA 0213B, 617-661-0072 circle no. 261, p. 54
Loughborough Sound Images Ltd., The Technology Centre, Loughborough, Leicestershire, England LE11 0QE, (44+509) 231 843 circle no. 262, **
MathSoft Inc., 201 Broadway, Cambridge, MA 02139, 617-577-1017 circle no. 263, p. 54
The MathWorks Inc., 21 Eliot St., South Natick, MA 01760, 508-653-1415 circle no. 264, p. 54
MicroWay Inc., P.O. 8ox 79, Kingston, MA 02364, 50B-746-7341 circle no. 265, p. 54
Momentum Data Systems, 1520 Nutmeg Place, Suite 108, Costa Mesa, CA 92626, 714-557-6884 circle no. 266, p. 54
National Instruments Corp., 6504 Bridge Point Parkway, Austin, TX 78730, 512-33B-9119 circle no. 267, p. 54
Saber Software Inc., 1B5 Alewife Brook Parkway, Cambridge, MA 02138, 617-876-7636 circle no. 268, **
Signal Technology Inc., 120 Cremona 0r., Goleta, CA 93117, 805-968-3000 circle no. 269, p. 54
Signix, 19 Pelham Island Rd., Wayland, MA 01778, 508-358-5955 circle no. 270, p. 54
Sonitech International Inc., 14 Mica Lane, Suite 208, Wellesley, MA 021B1, 617-235-6824 circle no. 271, p. 54
Speakeasy Computer Corp., 224 S. Michigan Ave., Suite 1250, Chicago, IL 60604, 312-427-2400 circle no. 272, **
Spectral Innovations Inc., 4633 Old Ironside 0r. #450, Santa Clara, CA 95054, 408-727-1314 circle no. 273, p. 54
Spectrum Signal Processing Inc., 460 Totten Pond Rd., 4th Flr., Waltham, MA. 02154, 617-890-3400 circle no. 274, **
Zola Technologies Inc., 6195 Heards Creek 0r. N.W., Suite 201, Atlanta, GA 30328, 404-843-2972 circle no. 275, **

ANALOG

A.B. Associates Inc., 348 Eckles 0r., Tampa, FL 33612, 813-932-9853 circle no. 276, **
Analogy Inc., 9205 S.W. Gemini 0r., Beaverton, OR 97005, 503-626-9700 circle no. 277, p. 62
BV Engineering, 2023 Chicago Ave., Suite B13, Riverside, CA 92507, 714-781-0252 circle no. 278, **
Cadence Design Systems Inc., 2475 Augustine 0r., Santa Clara, CA 95054, 408-727-0264 circle no. 279, p. 64
Contec Microelectronics USA Inc., 2010 N. First St., Suite 530, San Jose, CA 95131, 408-436-0340 circle no. 280, p. 62
Deutsch Research, 761 0eSoto 0rive, Palo Alto, CA 94303, 415-327-8677 circle no. 281, p. 62, 64
EESof Inc., 5601 Lindero Canyon Rd., Westlake Village, CA 91362, 818-991-7530 circle no.282, p. 62, 64
Electrical Engineering Software Inc., 4675 Stevens Creek 8lvd., Suite 200, Santa Clara, CA 95051 408-296-8151 circle no. 283, p. 62, 64
Hewlett-Packard Co., 8245 North Union 8lvd., Colorado Springs, CO 80901, 719-590-5812 circle no. 284, **
Intusoft, 2515 South Western Ave., Suite 203, San Pedro, CA 90734, 213-833-0710 circle no. 285, p. 60, 64
Mentor Graphics Corp., 8500 S.W. Creekside Place, 8eaverton, OR 97005, 503-626-7000 circle no. 286, p.60, 64
Meta-Software Inc., 1300 White 0aks Rd., Campbell, CA 95008, 408-371-5100 circle no. 287, p. 60
MicroSim Corp., 20 Fairbanks, Irvine, CA 92718, 714-770-3022 circle no.288, p. 60
Omation Inc., B01 Presidential Dr., Richardson, TX 75081, 214-231-5167 circle no. 289, p. 60, 64
DrCAD L.P., 3175 N.W. Aloclek 0r., Hillsboro, OR 97124, 503-690-9881 circle no. 290, p. 60
Spectrum Software, 1021 South Wolfe Rd., Sunnyvale, CA 94086, 408-73B-4387 circle no. 291, p. 64
Swiftlogic Inc., 5201 Great American Parkway, Suite 3220, Santa Clara, CA 95054, 408-562-5060 circle no. 292, **
Valid Logic Systems, 2820 Orchard Parkway, San Jose, CA 95134, 408-432-9400 circle no.293, p. 60, 64
Vamp Inc., 6753 Selma Ave., Los Angeles, CA 90028, 213-466-5533 circle no. 294, p. 60, 64
Viewlogic Systems Inc., 293 8oston Post Rd. West, Marlboro, MA 01752, 800-422-4660 circle no. 295, **

EDIF

Accel Technologies Inc., 6825 Flanders 0r., San 0iego, CA 92121, 619-554-1000 circle no. 296, p. 69
Aldec, 3525 0ld Conejo Rd., Suite 111, Newbury Park, CA 91320, 805-499-6B67 circle no. 297, .**
Analogy Inc., 9205 S.W. Gemini 0r., Beaverton, OR 97075, 503-626-9700 circle no. 298, p. 69
Apple Computer Inc., 20525 Mariani Ave., Cupertino, CA 95014, 40B-996-1010 circle no. 299, **
BP Microsystems, 10681 Haddington, Suite 190, Houston, TX 77043, 800-225-2102 circle no. 300, **
Cad Language Systems Inc., 15245 Shady Grove Rd., Suite 310, Rockville, M0 20850, 301-963-5200 circle no. 301, **
Cad Software Inc., 119 Russell St., Suite 6, Littleton, MA 01460, 508-4B6-9521 circle no. 302, **
Cadence Design Systems Inc., 555 River 0aks Parkway, San Jose, CA 95134, 408-943-1234 circle no. 303, p. 69
Cadix International Inc., 2301 Maitland Center Parkway, Suite 445, Maitland, FL 32751, 407-875-0007 circle no. 304, **
Calay Systems Inc., 16842 Von Karman Ave., Suite 100, Irvine, CA 92714, 714-863-1700 circle no. 305, **
Capilano Computing, 1168 Hamilton St., Suite 501, Vancouver, 8.C., V68 2S2, Canada, 604-669-6343 circle no. 306, **
Comdisco Systems Inc., 919 East Hillsdale 8lvd., Foster City, CA 94404, 415-574-5800 circle no. 307, **
Computer Timing Products Inc., 2705-160th Lane, N.E., Ham Lake, MN 55304, 612-434-8862 circle no. 308, p. 69
Computervision/A Prime Company, 100 Crosby 0r., Bedford, MA 01730, 617-275-1B00 circle no. 309, p. 69
Contec Microelectronics USA Inc., 2010 North First St., Suite 530, San Jose, CA 95131, 800-888-8884 circle no. 310, **
Cooper & Chyan Technology Inc., 5120 Campbell Ave., Suite 213, San Jose, CA 95130, 408-370-1481 circle no. 311, **
Dassault Electronique, 55 Qual Marcel 0assault, 92214 St.

** Not included in tables

Cloud, France, (33+1) 3481 6102 circle no. 312, **
Data I/O Corp., 10525 Willows Rd., N.E., Redmond, WA 98052, 206-881-6444 circle no. 313, p. 69
Dazix, 5775 Flatiron Parkway, Boulder, CO 80301, 303-444-8075 circle no. 314, p. **
Design Workshop, 4226 St. John's Blvd., Suite 400, Dollard Des Ormeaux, Quebec, Canada H9G 1X5, 514-696-4753 circle no. 315, **
Dosis GmbH, 1737 North 1st St., Suite 300, San Jose, CA 95112, 408-436-5740 circle no. 316, **
Electrical Engineering Software Inc., 4675 Stevens Creek Blvd., Suite 200, Santa Clara, CA 95051, 408-296-8151 circle no. 317, **
Emerald Design System Inc., 1043 North Shoreline Blvd., Mountain View, CA 94043, 415-965-3300 circle no. 318, **
Engineering DataXpress Inc., 5 Town and Country Village, Suite 736, San Jose, CA 95128-2026, 408-436-0403 circle no. 319, p. 69
EPIC Design Technology Inc., 2900 Lakeside Dr., Suite 205, Santa Clara, CA 95054, 408-988-2944 circle no. 320, **
Expert Views Inc., 175 Cabot St., Lowell, MA 01854, 508-970-0880 circle no. 321, **
formula GmbH, Spittlertorgraben 47, 8500 Nuremberg 90, Germany, (49+911) 28-6 600 circle no. 322, p. 70
Fujitsu Ltd., 3055 Orchard Dr., San Jose, CA 95134, 408-432-1300 circle no. 323, **
GenRad Inc., 300 Baker Ave., Concord, MA 01742, 508-369-4400 circle no. 324, p. 70
Harris Corp., Scientific Calculations Division, 7796 Victor Mendon Rd., P.O. Box H, Fishers, NY 14453, 716-924-9303 circle no. 325, **
Harris Semiconductor, 724 Rt. 202, P.O. Box 591, Somerville, NJ 08876, 201-685-6585 circle no. 326, **
Ikos Systems Inc. 145 North Wolfe Rd., Sunnyvale, CA 94086, 408-245-1900 circle no. 328, p. 70
i-Logix Inc., 22 Third Ave., Burlington, MA 01803, 617-272-8090 circle no. 327, **
Integrated Silicon Systems Inc., P.O. Box 13665, Research Triangle Park, NC 27709, 919-361-5814 circle no. 329, p. 70
Integrity Engineering Inc., 1306 West County Rd. S., Suite 100, St. Paul, MN 55112, 612-636-6913 circle no. 330, **
InterACT Corp., 417 Fifth Ave., New York, NY 10016, 212-696-3700 circle no. 331, **
Intergraph Corp., One Madison Industrial Park, Huntsville, AL 35894-0001, 205-730-8584 circle no. 332, p. 70
ISDATA Inc., 800 Airport Rd., Monterey, CA 93940, 408-373-7359 circle no. 333, p. 70
Knights Technology Inc., 3506 Bassett St., Santa Clara, CA 95054, 408-988-0600 circle no. 334, p. 70
Logic Automation, P.O. Box 310, Beaverton, OR 97075, 503-690-6900 circle no. 335, **
Logic Modeling Systems Inc., 1520 McCandless Dr., Milpitas, CA 95035, 408-957-5200 circle no. 336, **
Logical Devices Inc., 1201 N.W. 65th Place, Ft. Lauderdale, FL 33309, 305-974-0967 circle no. 337, p. 70
LSI Logic Corp., 1551 McCarthy Blvd., Milpitas, CA 95035, 408-433-8000 circle no. 338, **
Mentor Graphics Corp., 8500 S.W. Creekside Place, Beaverton, OR 97005, 503-626-1410 circle no. 339, p. 70
Meta-Software Inc., 1300 White Oaks Rd., Campbell, CA 95008, 408-371-5100 circle no. 340, **
MicroSim Corp., 20 Fairbanks, Irvine, CA 92718, 714-770-3022 circle no. 341, **
Microtel Pacific Research LTD (MPR), 8505 Eastlake Dr., Burnaby, B.C., Canada V5A 4T7, 604-421-3141 circle no. 342, **
National Semiconductor Corp., 2900 Semiconductor Dr., Santa Clara, CA 95051, 408-721-2650 circle no. 343, **
NCR Microelectronics Corp., 2001 Danfield Court, Ft. Collins, CO 80525, 303-226-9500 circle no. 344, **
NEC Electronics Inc., 401 Ellis St., Mountain View, CA 94039, 415-960-6000 circle no. 345, **
Omation Inc., 801 Presidential Dr., Richardson, TX 75081, 214-231-5167 circle no. 346, p. 70
OrCAD L.P., 3175 N.W. Aloclek Dr., Hillsboro, OR 97124, 503-690-9881 circle no. 347, p. 70
Pacific Numerix Corp., 1200 Prospect St., Suite 300, La Jolla, CA 92037, 619-587-0500 circle no. 348, **
Phase Three Logic Inc., 1600 N.W. 167th Place, Beaverton, OR 97006, 503-645-0313 circle no. 349, p. 70
Plessey Semiconductors, 1500 Green Hills Rd., Scotts Valley, CA 95066, 408-438-2900 circle no. 350, p. 70
Prime Computer Inc., 14952 N.W. Greenbrier Parkway, Beaverton, OR 97006, 503-645-2410 circle no. 351, p. 70
Quad Design Technology Inc., 1385 Del Norte Rd., Camarillo, CA 93010, 805-988-8250 circle no. 352, **
Quantic Labs Inc., 281 McDermot Ave., Suite 200, Winnipeg, Man. R3B 0S9, Canada, 204-943-2552 circle no. 353, **
Quickturn Systems Inc., 325 E. Middlefield Rd., Mountain View, CA 94043, 415-967-3300 circle no. 354, p. 70
Racal-Redac Inc., 1000 Wyckoff Ave., Mahwah, NJ 07430, 201-848-8000 circle no. 355, p. 70
Sancad, 4660 La Jolla Village Dr., Suite 500, San Diego, CA 92122, 619-535-4815 circle no. 356, **
Schlumberger CAD/CAM, 4251 Plymouth Rd., Ann Arbor, MI 48106, 313-995-6000 circle no. 357, **
Scientific and Engineering Software Inc., 1301 W. 25th St., Austin, TX 78705, 512-474-4526 circle no. 358, **
Seiko Instruments USA Inc., 1130 Ringwood Court, San Jose, CA 95131, 408-922-1907 circle no. 359, **
Silicon Automation Systems Inc., 1630 Oakland Rd., Suite A203, San Jose, CA 95131, 408-437-9161 circle no. 360, p. 70
Silvar-Lisco, 703 E. Evelyn Ave., Sunnyvale, CA 94086, 408-991-6000 circle no. 361, p. 70
Simucad Inc., 32970 Alvarado-Niles Rd., Suite 74, Union City, CA 94587, 415-487-9700 circle no. 362, **
Simutest Inc., 2320-J Walsh Ave., Santa Clara, CA 95051, 408-988-6550 circle no. 363, p. 71
Swiftlogic Inc., 5201 Great America Parkway, Suite 3220, Santa Clara, CA 95054, 408-562-6060 circle no. 364, **
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Technical Systems Integrators Inc. (TSI), 5762 S. Semoran Blvd., Orlando, FL 32822, 818-795-1696 circle no. 367, **
Teradyne EDA, 5155 Old Ironsides Dr., Santa Clara, CA 95054, 408-980-5200 circle no. 368, p. 71
Texas Instruments Inc., 8390 LBJ Freeway, Dallas, TX 75243, 214-997-2796 circle no. 369, **
Toshiba America Electronic Components Inc., 1220 Midas Way, Sunnyvale, CA 94086, 408-737-9844 circle no. 370, **
Trend Circuits Inc., 44358 Old Warm Springs Blvd., Fremont, CA 94538-6148, 415-651-1150 circle no. 371, **
TSSI, 8205 S.W. Creekside Place, Beaverton, OR 97005, 503-643-9281 circle no. 372, **
Valid Logic Systems, 2820 Orchard Parkway, San Jose, CA 95134, 408-432-9400 circle no. 373, p. 71
Vantage Analysis Systems Inc., 42840 Christy St., Suite 201, Fremont, CA 94538, 415-659-0901 circle no. 374, p. 71
Versatec, 2710 Walsh Ave., Santa Clara, CA 95052-8091, 408-988-2800 circle no. 375, **
Viewlogic Systems Inc., 293 Boston Post Rd. W., Marlboro, MA 01752, 800-422-4660 circle no. 376, **
VLSI Technology Inc., 1109 McKay Dr., San Jose, CA 95131, 408-434-3000 circle no. 377, **
Zuken America Inc., One Oak Park Dr., Bedford, MA 01730, 617-275-0700 circle no. 378, p. 71
Zycad Corp., 1380 Willow Rd., Menlo Park, CA 94025, 415-688-7400 circle no. 379, p. 71

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EESof Inc., 5601 Lindero Canyon Rd., Westlake Village, CA 91362, 818-991-7530 circle no. 381, p. 74
Hewlett-Packard Corp., 1400 Fountain Grove Parkway, Santa Rosa, CA 95403, 707-577-1400 circle no. 382, p. 74
IMSL, 2500 Permian Tower, 2500 CityWest Blvd., Houston, TX 77042, 713-782-6060 circle no. 383, **
Infolytica Corp., 1140 de Maisonneuve, Suite 1160, Montreal, Que., Canada H3A 1M8, 514-849-8752 circle no. 384, p. 74
Integrated Engineering Software Inc., 347-435 Ellice Ave., Winnipeg, Man., Canada R38 146, 204-942-5636 circle no. 385, p. 74
The MacNeal-Schwendler Corp., 9076 North Oearbrook Trail, Milwaukee, WI 53223, 414-357-8723 circle no. 386, p. 74
Pacific Numerlx, 1200 Prospect St., Suite 300, La Jolla, CA 92037, 619-587-0500 circle no. 387, p. 74
Quad Oesign Technology Inc., 1385 Oel Norte Rd., Camarillo, CA 93010, 805-988-8250 circle no. 388, p. 74
Quantic Laboratories Inc., 281 McOermot Ave., Suite 200, Winnipeg, Man. R380S9, Canada, 204-943-2552 circle no. 389, p. 74
Racal-Redac, 100 Wyckoff Rd., Mahwah, NJ 07430, 201-848-8000 circle no. 390, **
Sonnet Software, 101 Old Cove Rd., Liverpool, NY 13090, 315-453-3096 circle no. 391, p. 74
Swanson Analysis Systems Inc., P.O. Box 65, Johnson Rd., Houston, PA 15342, 412-746-3304 circle no. 392, p. 74
Vector Fields Ltd., 24 Bankside, Kidlington, Oxford OX5 1JE England, (44+86) 75 70 277 circle no. 393, p. 74
Vector Fields Inc., 1700 North Farnsworth Ave., Aurora, IL 60505, 312-851-1734 circle no. 394, **

CASE

Atherton Technology, 1333 Bordeaux Dr., Sunnyvale, CA 94089, 408-734-9822 circle no. 395, p. 80
Cadre Technologies Inc., 222 Richmond St., Providence, RI 02903, 401-351-CASE circle no. 396, p. 80
Code Farms Inc., 7412 Jock Trail, Richmond, Ontario, K0A 2Z0, Canada, 613-838-4829 circle no. 397, p.80
Hewlett-Packard Co., 3000 Hanover St., P.O. Box 10301, Palo Alto, CA 94303, 415-857-1501 circle no. 398, p. 80
i-Logix Inc., 22 Third Ave., Burlington, MA 01803, 617-272-8090 circle no. 399, p. 80
Index Technology Corp., One Main St., Cambridge, MA 02142, 617-494-8200 circle no. 400, **
Interactive Oevelopment Environments (IOE) Inc., 595 Market St., 10th Floor, San Francisco, CA 94105, 415-543-0900 circle no. 401, p. 80
Interactive Software Engineering Inc., 270 Storke Rd., Suite 7, Goleta, CA 93117, 805-685-1006 circle no. 402, p. 80
Mentor Graphics Inc., 8500 S.W. Creekside Place, Beaverton, OR 97005, 503-626-7000 circle no. 403, p. 80
Meta-Software Corp., 1300 White Oaks Rd., Campbell, CA 95008, 408-371-5100 circle no. 404, p. 80
MicroWay Inc., P.O. Box 79, Kingston, MA 02364, 508-746-7341 circle no. 405, p. 80
MIL 3 Inc., 3400 International Dr. N.W., Washington, D.C. 20008, 202-364-8390 circle no. 406, p. 80
NeuralWare Inc., Penn Center West, Building 4, Suite 227, Pittsburgh, PA 15276, 412-787-8222 circle no. 407
Object Oesign Inc., One New England Executive Park, Burlington, MA 01803, 617-270-9797 circle no. 408, **
Objectivity Inc., 800 El Camino Real, 4th Floor, Menlo Park, CA 94025, 415-688-8000 circle no. 409, p. 80
RR Software Inc., P.O. Box 1512, Madison, WI 53701, 608-276-6022 circle no. 410, p. 80
Saber Software Inc., 185 Alewife Brook Parkway, Cambridge, MA 02138, 617-876-7636 circle no. 411, p. 80
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(Continued on p. 101)

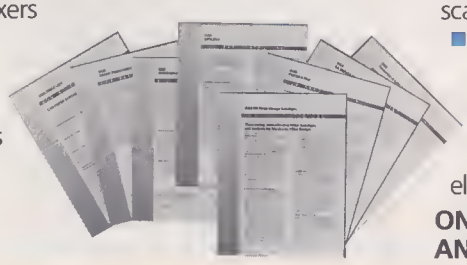
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INDEX

(Continued from p. 98)

Softool Corp., 340 South Kellogg Ave., Goleta, CA 93117, 805-683-5777 circle no. 413, p. 80
Software Research Inc., 625 Third St., San Francisco, CA 94107, 415-957-1441 circle no. 414, p. 80
Systems Control Technology Inc., 2300 Geng Rd., Palo Alto, CA 94303, 415-494-2233 circle no. 415, p. 80
TCI Software Research Inc., 1190 Foster Rd., Las Cruces, NM 88001, 800-874-2383 circle no. 416, p. 80
TeleSoft, 5959 Cornerstone Court West, San Diego, CA 92121, 619-457-2700 circle no. 417, p. 80
Mentor Graphics Corp., 1940 Zanker Rd., San Jose, CA 95112, 408-436-1500 circle no. 427, p. 82
MicroWay Inc., P.O. 8ox 79, Kingston, MA 02364, 508-746-7341 circle no. 428, **
Mihalisin Associates, 600 Honey Run Rd., Ambler, PA 19002, 215-646-3814 circle no. 429, **
OrCAD L.P., 3175 N.W. Aloclek Dr., Hillsboro, OR 97124, 503-690-9881 circle no. 430, p. 82
Quad Design Technology Inc., 1385 Del Norte Rd., Camarillo, CA 93010, 805-988-8250 circle no. 431, p. 84
Quantic Laboratories Inc., 281 McDermot Ave., Suite 200, Winnipeg, Man., Canada R38 0S9, 800-665-0235 circle no. 432, p. 84
Racal-Redac Inc., 238 Littleton Rd., Westford, MA 01886,
Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752, 508-481-3700 circle no. 443, p. 86
DSP Development Corp., One Kendall Square, Cambridge, MA 02139, 617-577-1133 circle no. 444, p. 88
Hyperception Inc., 9550 Skillman, Suite 302, Dallas, TX 75243, 214-343-8525 circle no. 445, p. 86, 88
Integral Signal Processing, P.O. Box 27661, Austin, TX 78755, 512-346-1451 circle no. 446, **
Jandel Scientific, 65 Koch Rd., Corte Madera, CA 94925, 415-924-8640 circle no. 447, p. 88
Keithley Asyst, 100 Corporate Woods, Rochester, NY 14623, 800-348-0033 circle no. 448, p. 86
Laboratory Technologies Corp., 400 Research Dr., Wilmington, MA 01887, 508-657-5400 circle no. 449, p. 86
...nc., 21 Eliot St., South Natick, MA 01760, circle no. 450, **
P.O. 8ox 79, Kingston, MA 02364, 508- circle no. 451, p. 88
...ates, 600 Honey Run Rd., Ambler, PA ·3814 circle no. 452, p. 88
...ents Corp., 6504 Bridge Point Parkway, 0, 512-794-0100 circle no. 453, p. 86
16440 Eagles Crest Rd., Ramona, CA ·5090 circle no. 454, **
...re Tools Inc., 30 East Swedesford Rd., 55, 215-889-1354 circle no. 455, p. 86
...Corp., 374 Maple Ave. East, Suite 200, .0, 703-281-3277 circle no. 456, **
...gy Inc., 120 Cremona Dr., Goleta, CA ·3000 circle no. 457, p. 86, 88
...nc., 3615 Harding Ave., Suite 505, Hon- 808-734-5801 circle no. 458, **
...uting Corp., 224 South Michigan Ave., 04, 312-427-2400 circle no. 459, p. 88
...Processing Inc., 460 Totten Pond Rd., 4th MA 02154, 617-890-3400 circle no. 460, p. 86
...Processing Inc., 3700 Gilmore Way, 8ur- ...da V5G 4M1, 604-438-7266 circle no. 461, p. 86

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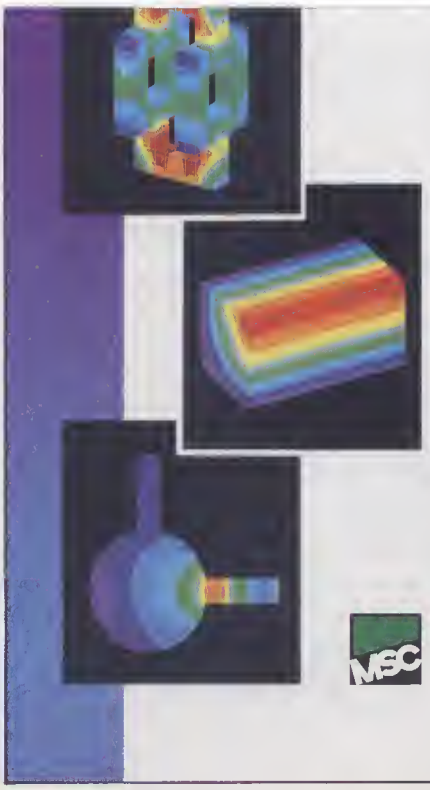
201 203 205 207 209 211 213 215 217 219 221 223 225 227 229 231 233 235 237 239 241 243 245 247 249
202 204 206 208 210 212 214 216 218 220 222 224 226 228 230 232 234 236 238 240 242 244 246 248 250

PRODUCT INFORMATION

251 262 273 284 295 306 317 328 339 350 361 372 383 394 405 416 427 438 449 460 471 482 493 504 515 526
252 263 274 285 296 307 318 329 340 351 362 373 384 395 406 417 428 439 450 461 472 483 494 505 516 527
253 264 275 286 297 308 319 330 341 352 363 374 385 396 407 418 429 440 451 462 473 484 495 506 517 528
254 265 276 287 298 309 320 331 342 353 364 375 386 397 408 419 430 441 452 463 474 485 496 507 518 529
255 266 277 288 299 310 321 332 343 354 365 376 387 398 409 420 431 442 453 464 475 486 497 508 519 530
256 267 278 289 300 311 322 333 344 355 366 377 388 399 410 421 432 443 454 465 476 487 498 509 520 531
257 268 279 290 301 312 323 334 345 356 367 378 389 400 411 422 433 444 455 466 477 488 499 510 521 532
258 269 280 291 302 313 324 335 346 357 368 379 390 401 412 423 434 445 456 467 478 489 500 511 522 533
259 270 281 292 303 314 325 336 347 358 369 380 391 402 413 424 435 446 457 468 479 490 501 512 523 534
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261 272 283 294 305 316 327 338 349 360 371 382 393 404 415 426 437 448 459 470 481 492 503 514 525 536

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Technical Systems Integrators Inc. (TSI), 5762 S. Semoran Blvd., Orlando, FL 32822, 818-795-1696 circle no. 367, **
Teradyne EDA, 5155 Old Ironsides Dr., Santa Clara, CA 95054, 408-980-5200 circle no. 368, p. 71
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Infolytica Corp., 1140 de Maisonneuve, Suite 1160, Montreal, Que., Canada H3A 1M8, 514-849-8752 circle no. 384, p. 74
Integrated Engineering Software Inc., 347-435 Ellice Ave., Winnipeg, Man., Canada R3B 1A6, 204-942-5636 circle no. 385, p. 74
The MacNeal-Schwendler Corp., 9076 North Oearbrook Trail, Milwaukee, WI 53223, 414-357-8723 RI 02903, 401-351-CASE circle no. 396, p. 80
Code Farms Inc., 7412 Jock Trail, Richmond, Ontario, K0A 2Z0, Canada, 613-838-4829 circle no. 397, p.80
Hewlett-Packard Co., 3000 Hanover St., P.O. Box 10301, Palo Alto, CA 94303, 415-857-1501 circle no. 398, p. 80
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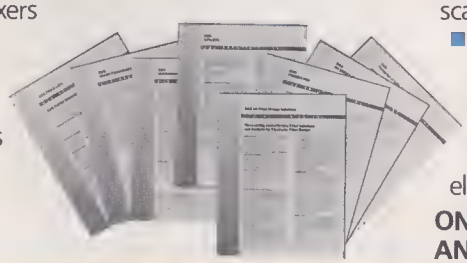
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INDEX

(Continued from p. 98)

Softool Corp., 340 South Kellogg Ave., Goleta, CA 93117, 805-683-5777 circle no. 413, p. 80
Software Research Inc., 625 Third St., San Francisco, CA 94107, 415-957-1441 circle no. 414, p. 80
Systems Control Technology Inc., 2300 Geng Rd., Palo Alto, CA 94303, 415-494-2233 circle no. 415, p. 80
TCI Software Research Inc., 1190 Foster Rd., Las Cruces, NM 88001, 800-874-2383 circle no. 416, p. 80
TeleSoft, 5959 Cornerstone Court West, San Diego, CA 92121, 619-457-2700 circle no. 417, p. 80
Texas Instruments Inc., 6550 Chase Oaks Blvd., MS 8474, Plano, TX 75023, 214-575-2130 circle no. 418, p. 80
Visible Systems Corp., The Bay Colony Corporate Center, 950 Winter St., Waltham, MA 02154, 617-890-2273 circle no. 419, **
Wintek Corp., 1801 South St., Lafayette, IN 47904, 800-742-6809 circle no. 420, **

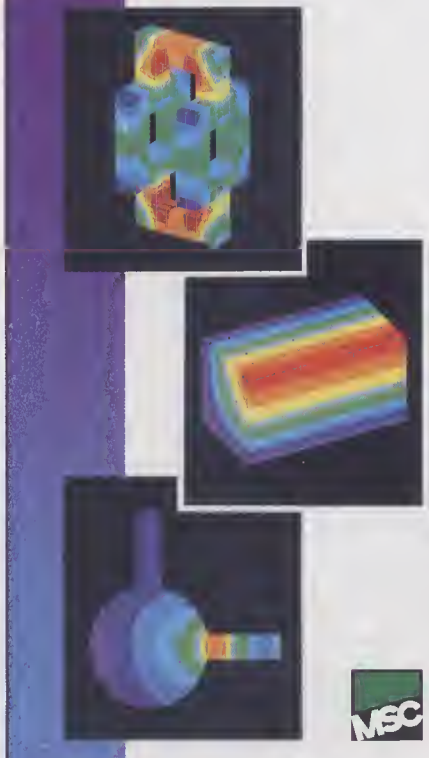
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Cadence Design Systems Inc., Advanced CAE Division, 2 Lowell Research Center Dr., Lowell, MA 01852, 508-458-1900 circle no. 425, p. 82
Hewlett-Packard Co., 3404 East Harmony Rd., Fort Collins, CO 80525, 303-229-3800 circle no. 426, p.82
Mentor Graphics Corp., 1940 Zanker Rd., San Jose, CA 95112, 408-436-1500 circle no. 427, p. 82
MicroWay Inc., P.O. Box 79, Kingston, MA 02364, 508-746-7341 circle no. 428, **
Mihalisin Associates, 600 Honey Run Rd., Ambler, PA 19002, 215-646-3814 circle no. 429, **
OrCAD L.P., 3175 N.W. Aloclek Dr., Hillsboro, OR 97124, 503-690-9881 circle no. 430, p. 82
Quad Design Technology Inc., 1385 Del Norte Rd., Camarillo, CA 93010, 805-988-8250 circle no. 431, p. 84
Quantic Laboratories Inc., 281 McDermot Ave., Suite 200, Winnipeg, Man., Canada R3B 0S9, 800-665-0235 circle no. 432, p. 84
Racal-Redac Inc., 238 Littleton Rd., Westford, MA 01886, 508-692-4900 circle no. 433, p. 82
Schlumberger CAD/CAM, 4251 Plymouth Rd., Ann Arbor, MI 48106, 313-995-6000 circle no. 434, p. 82
Swiftlogic Inc., 5201 Great America Parkway, Suite 3220 Santa Clara, CA 95054, 408-562-6060 circle no. 435, p. 84
Teradyne EDA, 5155 Old Ironsides Dr., Santa Clara, CA 95054, 408-980-5200 circle no. 436, p. 82
Valid Logic Systems, Two Omni Way, Chelmsford, MA 01824, 508-256-2300 circle no. 437, p. 84
Wintek Corp., 1801 South St., Lafayette, IN 47904, 800-742-6809 circle no. 438, **

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Burr-Brown Corp., 6730 South Tucson Blvd., Tucson, AZ 85706, 800-548-6132 circle no. 441, p. 88
BV Engineering Professional Software, 2023 Chicago Ave., Suite 813, Riverside, CA 92507, 714-781-0252 circle no. 442, p. 88
Data Translation Inc., 100 Locke Dr., Marlboro, MA 01752, 508-481-3700 circle no. 443, p. 86
DSP Development Corp., One Kendall Square, Cambridge, MA 02139, 617-577-1133 circle no. 444, p. 88
Hyperception Inc., 9550 Skillman, Suite 302, Dallas, TX 75243, 214-343-8525 circle no. 445, p. 86, 88
Integral Signal Processing, P.O. Box 27661, Austin, TX 78755, 512-346-1451 circle no. 446, **
Jandel Scientific, 65 Koch Rd., Corte Madera, CA 94925, 415-924-8640 circle no. 447, p. 88
Keithley Asyst, 100 Corporate Woods, Rochester, NY 14623, 800-348-0033 circle no. 448, p. 86
Laboratory Technologies Corp., 400 Research Dr., Wilmington, MA 01887, 508-657-5400 circle no. 449, p. 86
The MathWorks Inc., 21 Eliot St., South Natick, MA 01760, 508-653-1415 circle no. 450, **
MicroWay Inc., P.O. Box 79, Kingston, MA 02364, 508-746-7341 circle no. 451, p. 88
Mihalisin Associates, 600 Honey Run Rd., Ambler, PA 19002, 215-646-3814 circle no. 452, p. 88
National Instruments Corp., 6504 Bridge Point Parkway, Austin, TX 78730, 512-794-0100 circle no. 453, p. 86
Plotworks Inc., 16440 Eagles Crest Rd., Ramona, CA 92065, 619-457-5090 circle no. 454, **
Scientific Software Tools Inc., 30 East Swedesford Rd., Malvern, PA 19355, 215-889-1354 circle no. 455, p. 86
Signal Analytics Corp., 374 Maple Ave. East, Suite 200, Vienna, VA 22180, 703-281-3277 circle no. 456, **
Signal Technology Inc., 120 Cremona Dr., Goleta, CA 93117, 805-968-3000 circle no. 457, p. 86, 88
Soft Warehouse Inc., 3615 Harding Ave., Suite 505, Honolulu, HI 96816, 808-734-5801 circle no. 458, **
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Spectrum Signal Processing Inc., 460 Totten Pond Rd., 4th Floor, Waltham, MA 02154, 617-890-3400 circle no. 460, p. 86
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Strawberry Tree Inc., 160 South Wolfe Rd., Sunnyvale, CR 94086, 408-736-8800 circle no. 464, p. 86
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TriMetrix Inc., 444 NE Ravenna Blvd., Suite 210, Seattle, WA 98115, 206-527-1801 circle no. 466, p. 88
Zonic A&D Company, 25 Whitney Dr., Milford, OH 45150, 513-248-1911 circle no. 467, **

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Cadence Design Systems Inc., Advanced CAE Division, 2 Lowell Research Center Dr., Lowell, MA 01852, 508-458-1900 circle no. 472, p. 92
Compact Software, 483 McLean Blvd., Paterson, NJ 07513, 201-881-1200 circle no. 473, p. 92
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EESof Inc., 5601 Lindero Canyon Rd., Westlake Village, CA 91362, 818-991-7530 circle no. 479, p. 91, 92
EPIC Design Technology Inc., 2900 Lakeside Dr., Suite 205, Santa Clara, CA 95054, 408-988-2944 circle no. 480, p. 92
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Harris Corp., Scientific Calculations Division, 7796 Victor-Mendon Rd., P.O. Box H, Fishers, NY 14453, 716-924-9303 circle no. 482, p. 92
Hewlett-Packard Co., 8245 North Union Blvd., Colorado Springs, CO 80901, 719-590-5812 circle no. 483, **
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Mentor Graphics Corp., 8500 S.W. Creekside Place, Beaverton, OR 97005, 503-626-7000 circle no. 485, p. 92
Meta-Software Inc., 1300 White Oaks Rd., Campbell, CA 95008, 408-371-5100, circle no. 486, p. 91, 92
MicroSim Corp., 20 Fairbanks, Irvine, CA 92718, 714-770-3022 circle no. 487, **
Omation Inc., 801 Presidential Dr., Richardson, TX 75081, 800-553-9119 circle no. 488, **
DrCAD L.P., 3175 N.W. Aloclek Dr., Hillsboro, OR 97124, 503-690-9881 circle no. 489, **
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Quad Design Technology Inc., 1385 Del Norte Rd., Camarillo, CA 93010, 805-988-8250 circle no. 491, p. 91
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Sonnet Software, 101 Old Cove Rd., Liverpool, NY 13090, 315-453-3096 circle no. 495, p. 92
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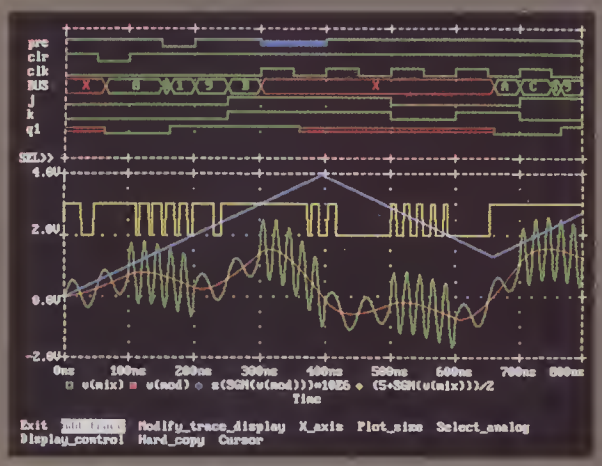
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DGS Associates Inc., 1353 Sarita Way, Santa Clara, CA 95051, 408-554-1469 circle no. 212, p. 98
Doctor Design, 5415 Oberlin Dr., San Diego, CA 92121, 619-457-4545 circle no. 219, p. 102
DSP Development Corp., One Kendall Square, Building 100, Cambridge, MA 02139, 617-577-1133 circle no. 210, p. 104
DSP Research, 391 Balsam Ave., Sunnyvale, CA 94086, 408-773-1042 circle no. 218, p. 66
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Integrated Systems Inc., 2500 Mission College Blvd., Santa Clara, CA 95054, 408-980-1500 circle no. 205, p. 56
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MacNeal-Schwendler Corp., 815 Colorado Blvd., Los Angeles, CA 90041, 800-MAG-6442 circle no. 227, p. 101
Meta-Software Inc., 1300 White Oaks Rd., Campbell, CA 95008, 408-371-5100 circle no. 201, p. 51
MicroSim Corp., 20 Fairbanks, Irvine, CA 92718, 714-770-3022 circle no. 207, p. 103
Microstar Laboratories, 2863 152nd Ave., N.E., Redmond, WA 98052, 206-881-4286 circle no. 215, p. 94
MIL 3 Inc., 3400 International Dr. N.W., Washington, D.C. 20008, 202-364-8390 circle no. 202, p. 67
Momentum Data Systems, 1520 Nutmeg Place, Suite 108, Costa Mesa, CA 92626, 714-557-6884 circle no. 225, p. 58
Signal Technology Inc., 120 Cremona Dr., Goleta, CA 93117, 805-968-3000 circle no. 226, p. 46
Soft Warehouse Inc., 3615 Harding Ave., Suite 505, Honolulu, HI 96816, 808-734-5801 circle no. 211, p. 97
Software Research (SR) Inc., 625 Third St., San Francisco, CA 94107, 415-957-1441 circle no. 206, p. 84
Stellar Software, P.O. Box 10183, Berkeley, CA 94709, 415-845-8405 circle no. 208, p. 72
Systems Control Technology Inc., 2300 Geng Rd., Palo Alto, CA 94303, 800-227-1910 circle no. 203, p. 53
3-D Visions Inc., 412 South Pacific Coast Highway, Suite 201, Redondo Beach, CA 90277, 213-540-8818 circle no. 224, p. 96
TransEra Corp., 3707 North Canyon Rd., Provo, UT 84604, 801-224-6550 circle no. 214, p. 63
Viewlogic Systems Inc., 293 Boston Post Rd. West, Marlboro, MA 01752, 800-422-4660 circle no. 223, p. 65
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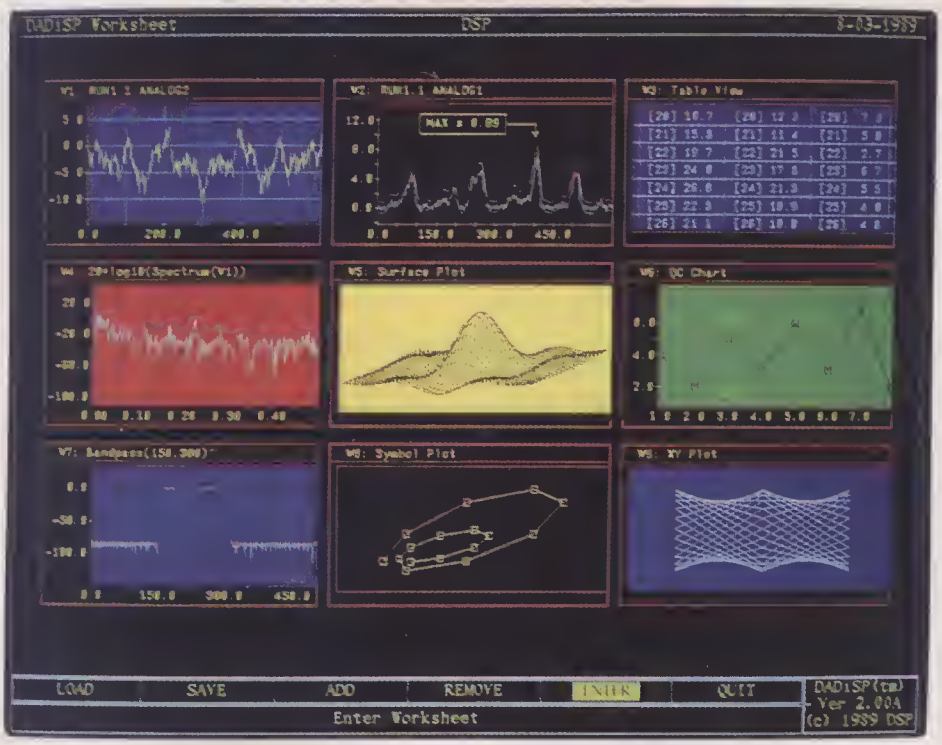
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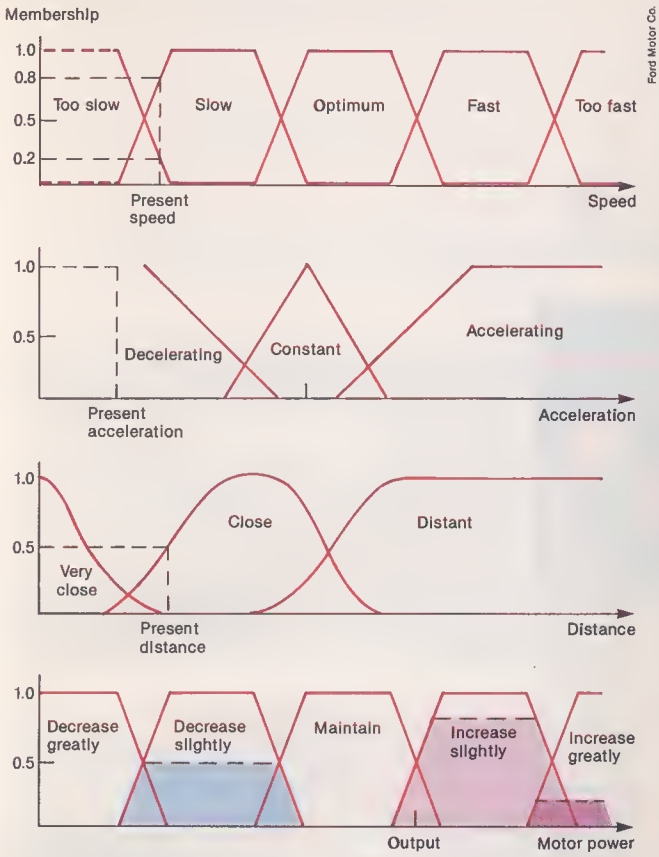
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Designing with fuzzy logic

(Continued from p. 44)



[2] An automatic controller for a vehicle provides a simple application of fuzzy set theory. Such a controller is designed to optimize travel time by monitoring speed and distance from a destination and reacting accordingly. Its three inputs are present speed, acceleration, and distance from the destination; its one output is motor power.

The vehicle is currently laboring ever more slowly up a steep hill. The membership functions assign linguistic variables to the inputs: acceleration, "decelerating"; distance, "close"—both with a weight of 1. The present speed is a member of the linguistic variable "slow" and "too slow," with weights of 0.8 and 0.2, respectively.

The rule set consists of several rules, but only three are shown executing here:

IF speed is TOO SLOW and acceleration is DECELERATING,
THEN INCREASE POWER GREATLY

IF speed is SLOW and acceleration is DECELERATING,
THEN INCREASE POWER SLIGHTLY

IF distance is CLOSE,
THEN DECREASE POWER SLIGHTLY

The confidence level of the result of any rule will be the minimum of the confidence levels of any of the input variables to that rule, causing the output to be "clipped." The centroid of the three areas is calculated to find the appropriate output of the system, in this case a moderate increase in power, because, although the vehicle is slowing on the hill, the destination is near.

The Fuzzy VME Accelerator board is priced at US $4500, and the FC110 processor alone sells for US $80 when purchased in quantities of 1000.

The largest consortium for fuzzy research is the Laboratory for International Fuzzy Engineering (Life), Yokohama, which was organized by the Japan Ministry of International Trade and Industry (MITI). It boasts an impressive membership of 45 companies from Japan and Japanese subsidiaries of U.S. and European companies, including Hitachi Ltd., Sony Corp., IBM Japan, and Thomson Japan K.K, and is planned to continue until at least 1995. With a proposed budget of 5 billion yen (US $35 million), Life is conducting basic research on fuzzy control and information processing with universities and member companies, with intellectual property to be owned jointly by Life and its consortium members.

In the United States, the business community is beginning to take note. Fuzzy Venture Partners of Santa Monica, Calif., has formed the Fuzzy Venture Partners Fund, a US $70 million limited-partnership, specialty venture-capital fund. Aimed at start-up companies, the fund provides financial support and expertise to entrepreneurs involved in the development of fuzzy systems. Limited-partnership interests start at US $2 million.

Fields of expertise

Although the applications listed here have concentrated on more traditional control approaches, fuzzy logic is very powerful in fields such as expert systems, decision-making, and information processing. A program employed by Tokyo's Yamaichi Securities Co., uses fuzzy decision-making to manage a 50 billion yen (US $350 million) stock market portfolio. The Sony PCT-500 handheld computer uses a fuzzy recognition system to interpret over 3000 handwritten Japanese characters as input. Retailing for 198 000 yen (US $1400), it eliminates the need for a large and cumbersome keyboard. In the United States, research is being conducted by the National Aeronautics and Space Administration into the use of fuzzy logic to dock spacecraft, reducing the possibility of human error.

Undoubtedly, fuzzy logic is a fast, cost-effective method for automated control in many systems. Products designed with fuzzy logic boast simpler, more user-friendly controls, are easier to construct and test, and offer smoother control than those using traditional systems. While it has been slow to be adopted outside of Japan, its wide-ranging applicability ensures it increasing importance as a method of system control.

The fuzzy future

"The primary barrier to the use of fuzzy logic is a psychological one, not a commercial one," observed Camerone Welch of the Gartner Group Inc., a technology-related information service company that is located in Stamford, Conn. "There is a big reluctance to use it until someone in the U.S. market proves it can work, like an IBM or DEC. When that happens, fuzzy technology will take the United States like it has Japan, and the people who are prepared will cash in."

To probe further

Numerous journals and papers deal with fuzzy theory and applications. Major periodicals in the field include the *International Journal of Fuzzy Sets and Systems*, and North American Fuzzy Information Processing Society's *International Journal of Approximate Reasoning*, edited by James Bezdek of the University of West Florida. Both are published in Amsterdam, the Netherlands, by North-Holland.

Fuzzy Sets and Applications: Selected Papers by L. A. Zadeh (ed. R.R. Yager et al., John Wiley & Sons, New York, 1987) provides a good overview of fuzzy set theory. The application of fuzzy systems to industrial control is discussed in *Industrial Applications of Fuzzy Control* by Michio Sugeno, published by North-Holland of Amsterdam. Current work combining the fields of fuzzy logic and neural networks is described by Bart Kosko in *Neural Networks and Fuzzy Systems* (Prentice-Hall, Englewood Cliffs, N.J., 1990).

The author gratefully acknowledges the assistance of the late Sam Bedrosian, professor of electrical engineering at the University of Pennsylvania in Philadelphia, who provided material for this article. ◆

How to select a microcontroller

Word length, input/output requirement, and the economics of on- and off-chip memory are among the factors to be weighed



To most of the world, the microcontroller is an unseen workhorse embedded in automobiles, microwave ovens, guided missiles, talking dolls, and a myriad of other applications. Unlike microprocessors, which are designed for a broad range of applications, microcontrollers are generally designed with a specific application in mind.

For the designer of an embedded system, however, the choice of a microcontroller is the earliest and probably the most important to be made. Delivering the final product on schedule, within budget, and to specification will depend heavily on making the right decision.

But how best to decide? This set of guidelines is for the neophyte designer to use as a checklist for evaluating candidate devices. And even experienced designers may discover in it selection criteria they have overlooked.

A microcontroller is generally dedicated to a single application and embedded in it. Unlike a microprocessor, it tends to include all of the peripheral features needed to implement the computer portion of an embedded application. Because their application constraints are known at the time of design, the designer is able to select the lowest-cost controller that can do the job. (By contrast, microprocessors usually wind up in general-purpose computers whose final use is not known in advance to their designers.)

Bounding the problem

The first decision to make is the level of performance required, that, on the word size of the controller. Those available can be grouped broadly as 4-, 8-, 16- and 32-bit products.

Standard benchmarks of the type used to describe microprocessors are inappropriate for this evaluation. They must be replaced by critical real-time calculations and physical constraints peculiar to the system being designed. Critical calculations are those that, if not completed within a specified period of time, cause the system to lose synchronization, create a dangerous situation, or generate wrong results. For instance, if a simple timer is to generate a square wave of a given frequency, the central processing unit (CPU) must be fast enough to calculate the time at which each edge should occur and to program the timer appropriately.

Physical constraints imposed by the system, such as precision and dynamic range, determine CPU class. For instance, a numerically controlled machine might require a relative accuracy of 1 degree within a single revolution of an axis. For this accuracy, an 8-bit data value, which can resolve no more than 1 part in 256, is inadequate, whereas a 16-bit data value will represent 1 part in 65 536, or about 20 seconds of arc.

Dynamic range further constrains the system. If the same machine must also be able to provide an absolute accuracy of 1 degree over 1000 revolutions of a lead screw, even 16 bits cannot represent the full range. In such a case, the designer could choose a 32-bit solution or, if extremely wide dynamic range is necessary, resort to a floating-point number system.

The designer is cautioned, however, that choosing a CPU on the basis of a single calculation could be a mistake. If the application generally requires lower-resolution calculations, it may be better to select a processor that matches just the predominant operations, while performing the higher-resolution calculations in subroutines. In most applications, for example, a good floating-point math package is superior to floating-point hardware.

The second step—the most often overlooked—is to identify the quantity, frequency, and type (analog, digital, serial, and so on) of all input/output (I/O) signals, as well as any other special requirements, including those imposed by mechanical aspects of the system. Key to this part of the selection process is a complete top-level block diagram of the overall system. Although it is not important to assign microcontroller peripheral functions at this stage, a preliminary partitioning might be helpful in identifying system requirements.

The third consideration is the application's memory requirements, which should be further broken down into program memory and data memory. Microcontroller memory may be categorized broadly as volatile and nonvolatile. Volatile random-access memory (RAM) retains data only while power is applied; it is generally used for data memory. Nonvolatile read-only memory (ROM) retains its contents permanently; it typically contains the

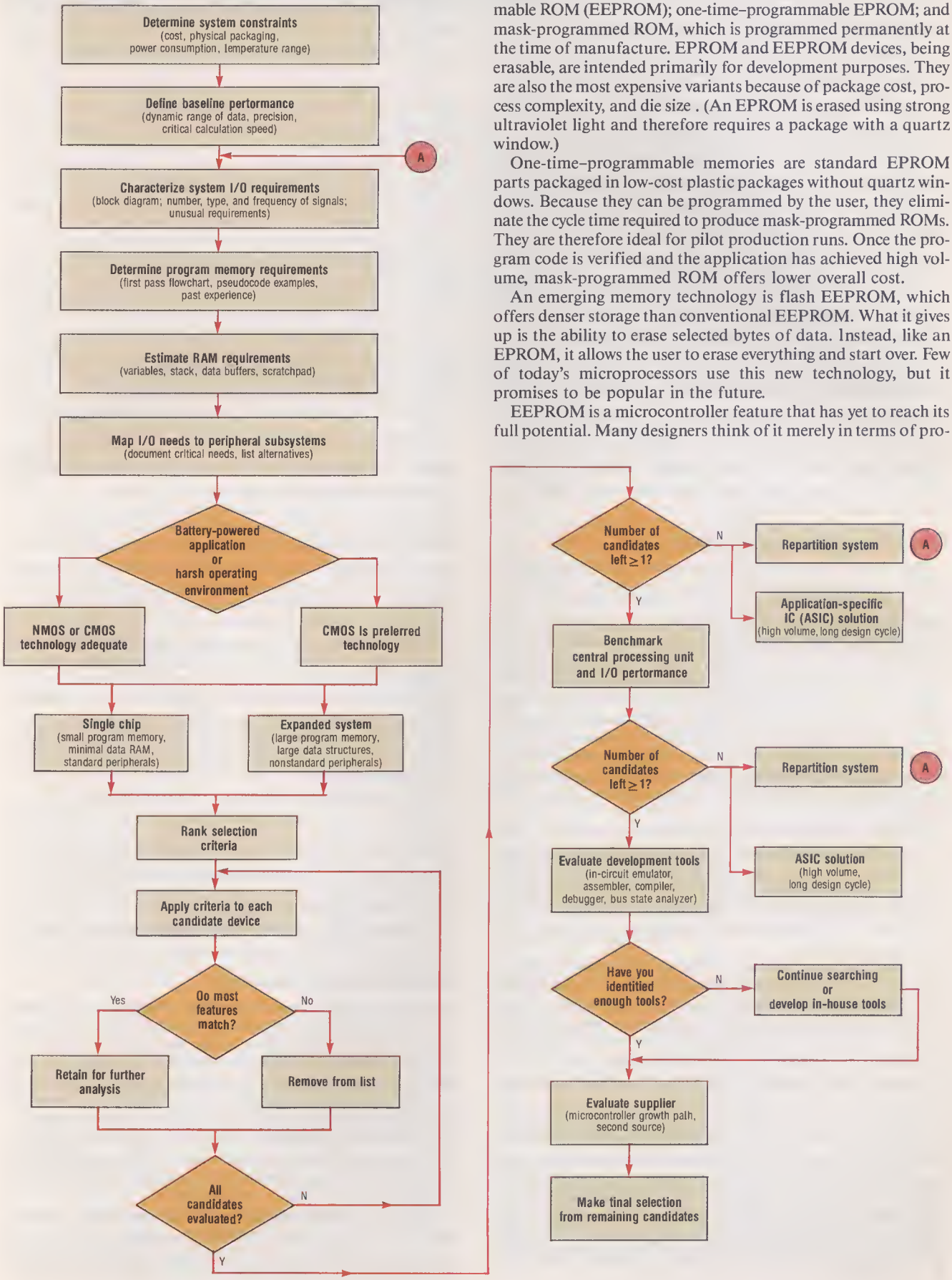
Defining terms

Benchmark: a standardized test or suite of tests for comparing computer performance; also, the act of determining a benchmark.
Dynamic range: the ratio of the largest to the smallest values of a range, often expressed in decibels.
Embedded system: a system into which one or more computing devices (which may be microprocessors or microcontrollers) are incorporated in such a way that the embedded device or devices are not directly accessible to the user of the system.
Floating point: the representation of numbers in scientific notation, with the exponent and mantissa given separately, so as to be able to accommodate a very wide dynamic range.
Mask-programmed: said of a semiconductor device, most often a read-only memory, that is permanently programmed as a step in its manufacture. In contrast, "field-programmed" applies to memory devices that are programmed after manufacture.
NMOS: n-channel metal-oxide-semiconductor, a type of MOS field-effect transistor.
RFI: Radio-frequency interference. (Usually) unintentionally radiated electromagnetic energy that may interfere with the operation of, or even damage, electronic equipment.

John J. Vaglica and Peter S. Gilmour Motorola Inc.

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Steps in selecting a microcontroller



application program of the embedded system.

Nonvolatile memory comes in four variants: electrically programmable ROM (EPROM); electrically erasable/programmable ROM (EEPROM); one-time–programmable EPROM; and mask-programmed ROM, which is programmed permanently at the time of manufacture. EPROM and EEPROM devices, being erasable, are intended primarily for development purposes. They are also the most expensive variants because of package cost, process complexity, and die size . (An EPROM is erased using strong ultraviolet light and therefore requires a package with a quartz window.)

One-time–programmable memories are standard EPROM parts packaged in low-cost plastic packages without quartz windows. Because they can be programmed by the user, they eliminate the cycle time required to produce mask-programmed ROMs. They are therefore ideal for pilot production runs. Once the program code is verified and the application has achieved high volume, mask-programmed ROM offers lower overall cost.

An emerging memory technology is flash EEPROM, which offers denser storage than conventional EEPROM. What it gives up is the ability to erase selected bytes of data. Instead, like an EPROM, it allows the user to erase everything and start over. Few of today's microprocessors use this new technology, but it promises to be popular in the future.

EEPROM is a microcontroller feature that has yet to reach its full potential. Many designers think of it merely in terms of pro-

gram storage, not as a strategic peripheral. However, it can do much more. For example, in an application developed in the computer peripheral industry, mechanical and electrical adjustments traditionally implemented with set screws and potentiometers were replaced with parameters stored in EEPROM.

Additional locations in the EEPROM store the date of manufacture, model and serial numbers, and other data describing the product. Warranty service can make use of the information stored in the product during manufacture, as well as additional data gathered during field operation.

Estimating the amount of memory to allocate for program storage will be one of the tougher parts of the selection process. There is no magical rule of thumb. Past experience coupled with a first-pass flowchart and pseudocode examples are likely to be the most appropriate available tools. Simple applications, such as electronic thermostats, may require as few as 2K bytes, while complex applications, such as engine controls, may require 64K or more.

Sufficient RAM must be allocated in the system to store variables, the system stack frame, a scratchpad for intermediate calculations, and any data arrays or buffers. These values will be affected by the programming language used to develop the application (system stack), the selected partitioning of the problem (variables), and even the hardware configuration (data buffers). Preliminary estimates for variable stack and scratchpad storage are often done by taking a percentage of the ROM estimate. The rule of thumb used by the authors is a ROM to RAM ratio in the range of 12–20:1. Applications written in assembly language will tend toward the lower number, while compiled code will require the higher amounts. Large data buffers should be added to this estimate.

Mapping I/O to peripherals

Peripheral functions commonly integrated on microcontrollers include timers, serial and parallel communications ports, and analog-to-digital (A/D) converters. Timers range from simple counters to complex subsystems with dedicated microengines incorporating reduced–instruction-set computer (RISC) architecture. Timer systems are commonly called upon to generate periodic interrupts, capture the time an input event occurs, or generate output events at specified times. The more complex timers can produce the pulse trains required of multiphase stepper motors or even of sequencing the fuel injectors in an automobile engine without CPU intervention. The frequencies of the input and output signals generally dictate how timer complexity should be traded off against the CPU overhead required for servicing the peripheral.

External peripherals added to provide functions not usually found on microcontrollers may be interfaced through either a parallel (address, data and control) bus or a serial port. The parallel bus is conceptually simple, but fraught with many practical problems because of its rapid switching of many data lines. It generates a lot of radio frequency interference (RFI), and it consumes a lot of power.

For applications that would be handled by a single chip except for a single special function, it is best to add the peripheral via a serial bus. Only two or three pins are required, RFI is generated only during serial transmissions, and power consumption rises only slightly. A variety of chips that perform peripheral functions are marketed with serial interfaces. Among them are A/D converters, phase-locked loop (PLL) building blocks, real-time clocks, display drivers, and EEPROMs.

Parallel I/O can be found on virtually all microcontrollers, but the ports are not all equivalent. The more versatile permit pins to be defined as input or output on a per-bit basis. That can be important if system parameters are subject to change before the design is complete (as is usually the case). Other, less flexible designs offer fixed direction, input-only, or output-only pins. Beware also of manufacturers' claims for large numbers of I/O pins, which in reality are available only if all the other on-chip peripherals are disabled.

A/D converters are found on many microcontrollers. Converters with 8- or 10-bit ranges are most common, but not all manufacturers offer the same resolution for a given range. The specsmanship issues that apply to stand-alone A/D converters are an even bigger problem with converter ICs. If the intended purpose is much more demanding than checking battery voltage, care must be taken to examine all the specifications of this subsystem.

An application that seems to require a unique peripheral may not after all, for it is often possible to minimize cost by using available peripherals in innovative ways. Digital-to-analog (D/A) converters, for example, are seldom integrated into microcontrollers. When one is needed, however, the resourceful engineer will provide one economically by integrating a pulse-width–modulated waveform generated by an on-chip timer. The integrator can be as simple as a passive RC low-pass filter.

Peripherals requiring frequent interrupt service consume valuable CPU bandwidth. Several methods employed by microcontroller designers reduce interrupt overhead. Unique vectors for each interrupt source, multiple priority levels, and hardware priority resolution circuits eliminate software polling of interrupt sources. Interrupt-driven direct-memory-access (DMA) peripherals transfer data with minimal CPU service overhead, although they still require considerable bus bandwidth. Other designs get rid of service requirements altogether by distributing enough intelligence to the peripheral to eliminate CPU servicing completely during normal operation.

Bus bandwidth is affected by two components: bus width and transfer rate. Boosting either causes a corresponding increase in bandwidth. Unfortunately, this bandwidth increase normally implies a cost increase as well. Microcontroller architects have designed features into high-end products that minimize the effect of greater bandwidth on system cost. Seldom will all memory and peripherals in a system need to be accessed at the highest possible rate. Infrequently accessed devices can be replaced with lower-cost, slower devices if wait state capabilities have been designed into the bus structure.

Microcontrollers with dynamically sized buses permit memories of different widths to coexist on the same bus. Resources requiring high bandwidth, such as the stack RAM, can occupy the full bus width. Locations accessed less often, such as the boot ROM, can be configured for the width of a single memory part. Reducing the number of devices by means of dynamic sizing minimizes use of printed-circuit board area, increases reliability, and decreases RFI.

Cost, packaging, operating environment, and other physical conditions further constrain the designer. These constraints must be spelled out clearly early on, for they bear directly on the microcontroller selected. Power consumption and temperature range dictate the processing technology(ies) suitable for the application. If the product is battery powered or will operate over an extended temperature range, a CMOS version would be the better choice. For an application in which these criteria are less important, an NMOS processor could offer a cost advantage.

Single-chip or expanded?

Microcontrollers often support multiple modes of operation for a better match to the application at hand. The two most common modes are single-chip and expanded. In the first of these, all aspects of the computer are contained on the microcontroller chip. The address, data, and control buses required for memory or peripheral expansion are not brought out to pins. In the expanded mode, these buses are made available. Microcontrollers capable of both single-chip and expanded modes fit well in applications where future upgrades or cost reductions are likely and a consequent complete rewrite of the application software undesirable.

Choosing between a single- and multi-chip solution depends heavily on memory size. Technology currently limits on-chip memories to 32K bytes for program (nonvolatile) storage and 1–2K bytes for data RAM. Otherwise, an expanded system using

Common microcontroller peripheral functions and their applications

Function	Automotive	Consumer	Computer peripheral
4-, 8-bit central processing unit (CPU)	Radio	Microwave oven	Keyboard
16-bit CPU	Antilock brake system	Audio	Disk drive
32-bit CPU	Engine control	—	Intelligent disk controller
Electrically erasable/programmable ROM	Odometer	Television channel programming	Modem configuration parameters
Timer	Fuel injection timing	Camera shutter speed	Mouse optical shaft encoder
Asynchronous serial	Communication throughout car	Alarm system keypad communication	RS232 link for modem
Synchronous serial	Vacuum fluorescent driver interface	Audio interchassis communication	Real-time clock interface on PC
Analog/digital converter	Manifold air pressure (engine control)	Temperature sensor for air-conditioning thermostat	Battery voltage for portable PC
Parallel I/O	Dashboard lamp driver	Videocassette recorder front panel switches	Status lights on keyboard

external memory ICs will be needed.

The distribution of on-chip versus external memory can affect total IC cost significantly. Since memories are only available in a limited range of sizes and on-chip memories are more expensive (on a per-bit basis) than external memory, it may be advantageous to move all program and/or data memory off chip in exchange for a less expensive microcontroller chip. Several manufacturers offer microcontrollers with little or no on-chip memory for this very reason.

In addition to memory size, other obvious factors that affect the single-chip vs. multi-chip decision are power consumption, peripheral mix, and cost. But there are also less obvious factors. For instance, microcontroller-generated RFI is a major concern in RF communication applications. High-speed digital outputs contribute significant energy to the radio spectrum. Confining these signals on chip, where capacitive loads and signal line lengths are reduced up to 100 times, significantly reduces emission levels. Realizing the problems that high-frequency signals cause, some microcontroller designers have gone so far as to provide software-programmable disables on potentially unused high-speed outputs.

The selection process

During the initial search, an absolute match between requirements and features is not necessary. Minor alterations to the requirements or the addition of a peripheral chip could create the most cost-effective solution from a less-than-perfect pairing.

The feature evaluation process should begin with a ranking of the requirements in order of descending priority, as determined by the application. If any requirements were not mapped to peripheral functions during the partitioning for the block diagram, they should be mapped at this point. This mapping will not restrict the selection to a particular device or manufacturer, but will identify the microcontroller features sufficiently for the selection process to progress. The designer is cautioned that devices may surface during the selection process that would be a perfect fit if only the system had been partitioned differently. An open mind will permit these possibilities to emerge.

The procedure at this stage is to compare each candidate microcontroller with the peripheral mapping and other requirements, retaining for further study any devices that match most of the requirements. If none is appropriate, the questions to ask are: Which criteria caused the most problems in finding a match? Could the offending requirements be altered? If not, would a repartitioning of the problem alleviate them? Several iterations may be necessary at this stage before a suitable chip or chips are found.

The first lists are sifted by applying more stringent criteria at each stage. For instance, after the field has been narrowed to a handful of candidates, actual application code sequences will be written and used to benchmark CPU performance. If undertaken before the list was narrowed, this step would drag out the evaluation inordinately.

An established growth path could be an important evaluation point if a family of products is planned. Many vendors offer microcontroller families built around a common CPU core where different family members feature different I/O and memory mixes. CPU performance improvements are made through clock frequency increases and upgrades to the core.

The final selection criteria are nontechnical. Potential vendors should be qualified after considering the following criteria: product line breadth, manufacturing excellence, financial status, second-sourcing strategy, and delivery performance. Development tools must also be taken into account. If inadequate, they could place the entire project in jeopardy; therefore, it is advisable to spend some time understanding what is available for the microcontroller chosen. The entry cost of development tools can be high.

Microcontroller selection is an arduous task entailing an inordinate number of decisions. There is no universal checklist that the designer can follow, only suggestions and guidelines. Experience, in fact, is the second most useful tool the designer can possess; the most useful is a well-defined set of system requirements. Without a list, an already difficult task becomes almost impossible.

To probe further

A good basic book is *Design with Microcontrollers*, by John B. Peatman (McGraw-Hill, 1988). It begins with an overview of microcontroller applications and goes on to explore the variety of available on-chip resources. Real-time control, the main use, is developed in depth.

Real-Time Microcomputer System Design: An Introduction, by Peter D. Lawrence and Konrad Mauch (McGraw-Hill, 1987), should be useful to practicing engineers and scientists working in the physical, biological, and applied sciences. It presents a methodology for the design of real-time microcomputer systems.

IEEE Micro magazine regularly publishes articles on new microcontroller and microprocessor products. The articles are generally written by the product designers and can provide information not generally available.

Embedded Systems Programming magazine is dedicated primarily to the software-related aspects of embedded-system design.

About the authors

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Are you ready for next-generation dynamic RAM chips?

Chip designers must evaluate tradeoffs such as stacked versus trench capacitors and consider the need to minimize power consumption



Dynamic random-access memories (DRAMs) are the simplest, and hence the smallest, of all semiconductor memories, containing only one transistor and one capacitor per cell. For that reason they are the most widely used memory type wherever high-density storage is needed, most obviously as the main memory in all types of computers. Static RAMs are faster, but their much larger cell size (which holds up to six transistors) keeps their densities one generation behind those that DRAMs can offer.

DRAM density has increased dramatically since the first 1K-bit units were introduced in 1970. Today, 1M-bit DRAMs are being produced in large quantities, and 4M-bit devices are available for the latest computers. Looking to the future, we see more powerful computers requiring even higher-density DRAMs.

Why?

There are two main reasons behind the demand for higher density: performance and size. It is generally agreed that a computer's memory size should grow in proportion to its speed if that speed is to be used effectively. A common rule of thumb is that the memory capacity in megabytes should equal about four times the processor speed in millions of instructions per second (MIPS). However, it is not acceptable to increase memory size by simply putting increasing numbers of low-density chips into a machine. Reliability would suffer.

To keep overall system reliability at an acceptable level, the total number of chips in any electronic system must be limited. Today, the limiting number is about 10 000 chips. Therefore, using today's 1M-bit chips, about a gigabyte of main memory can be realized. More than that would require higher-density RAMs.

Of more immediate importance today is the impact of chip density on computer size. The latest workstations are capable of performing at more than 10 MIPS, which means their ideal memory size is more than 40 Mbytes. It is impossible to build such machines in a desktop or laptop configuration with today's 1M-bit DRAMs. Using 4M-bit DRAMs, however, a laptop workstation has been made with such performance. It uses a reduced-instruction-set computer (RISC) chip as its central processor, has 40 Mbytes of DRAM, and delivers 13.5 MIPS.

But that's just for today. In a few years, computer power will increase by a factor of at least four, and then 16M-bit DRAMs will be required. And it will certainly be no more than five years before a need for 64M-bit DRAMs arises. How will those needs be met? Let's take a look.

The array noise problem

Historically, each generation of DRAMs has had four times the capacity of its predecessor. That quadrupling has been achieved mainly by reducing the sizes of the individual memory cells within the array. Each generation has had a cell size only one-third that of its predecessor. In addition, its chip size has been about 1.5 times larger. Between them, those two factors have accounted for the density increases.

As cells have shrunk in size over the years, various problems have arisen and been dealt with. Old timers may recall that the 64K-bit DRAM suffered in its early days from soft errors caused by alpha particles. That problem was solved in three main ways: by choosing packaging and other materials that did not produce alpha particles; by coating the chips with a polyimide layer to protect them from the particles; and, in some cases, by introducing a minority-carrier barrier layer below the cell capacitor.

For the 4M-bit generation, the main problem was getting enough capacitance for each cell. The solution was to adopt three-dimensional capacitor structures.

For 16M bits and beyond, noise looms as one of the main problems to overcome. As cell sizes get smaller, the bit lines (data lines) get closer together, and the capacitance grows between bit lines. As the capacitance goes up, coupling between bit lines increases, which means that each bit line is increasingly affected by the operation of its neighboring lines. Eventually a point is reached at which cell data cannot be read reliably because of that interference.

Several techniques have been proposed to reduce bit line interference noise. Researchers at Tokyo's Mitsubishi Electric Corp., for example, have proposed a twisted bit line approach, which would work in much the same way as twisted-pair wiring does in communications installations. Bit lines would be twisted with their complements. Noise coupled into such a pair would affect the two lines equally, thus effectively canceling itself.

An alternative approach, from Tokyo's Fujitsu Ltd., involves shielding the bit lines from each other by placing the cell capacitor between them.

Both methods have some disadvantages. The twisted bit line technique may require that an additional interconnection layer be added to accommodate the crossover wires, or it may impose a chip size penalty. The shielding approach would probably require more complex chip processing. Such difficulties notwithstanding, some steps must be taken to reduce this type of array noise in 64M-bit DRAMs.

Supply voltages for all DRAMs have always been 5 volts, and

Fujio Masuoka Toshiba Corp.

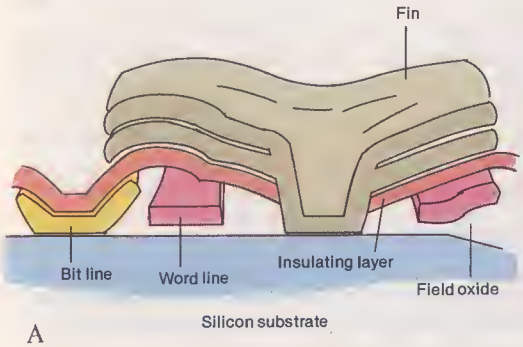
Defining terms

Array noise: unwanted disturbance in a memory IC generated by the normal movement of data within the array.
Punch-through: a disruptive discharge through a dielectric layer caused by the application of an excessive electric field.
Refresh cycle: the periodic recharging of the capacitors in a dynamic RAM (DRAM) array.
Storage node: the structure in a DRAM cell on which the cell's charge is stored; also called a storage electrode.

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are expected to remain there. However, starting with the 16M-bit DRAM, that externally supplied voltage will be reduced by on-chip conversion circuitry to 3 or 4 V for use by the actual memory elements. That reduction will both reduce chip power consumption and enhance reliability.

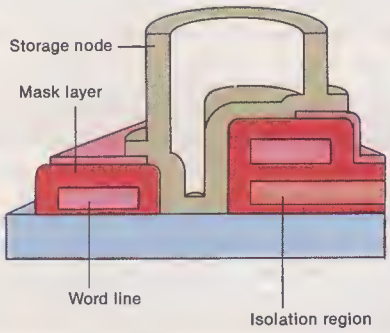
The largest item in the power budget of a DRAM is the precharging and discharging of the bit lines. Therefore, power consumption goes up with chip density as the number of bit lines activated in each cycle becomes larger. To keep the power consumption from exceeding the dissipation capabilities of standard plastic packages (about 500 milliwatts), two steps can be taken: lowering the bit line voltage and reducing the number of bit lines activated in one cycle (which, of course, requires increasing the number of cycles). Of the two, on-chip lowering of the voltage



A

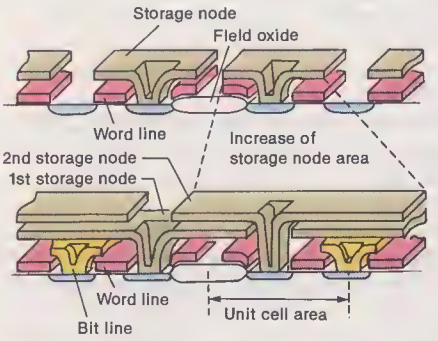


Fujitsu Ltd



B

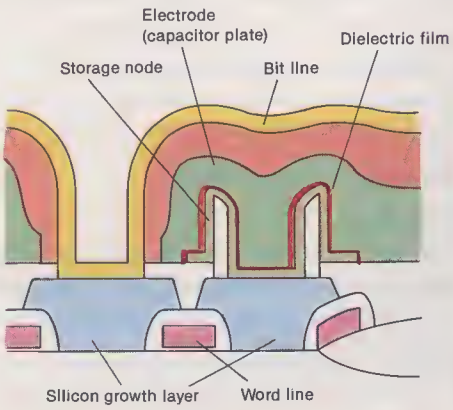
Fujitsu Ltd.'s fin-structured cell [above, left and right, A] is one method of increasing the capacitance of a stacked capacitor; it has a storage node formed by two polysilicon layers (fins) and two gaps. Mitsubishi Electric Corp.'s cylindrical cell approach [left, B] increases the capacitance of a stacked capacitor by increasing its height. Toshiba Corp.'s Spread Stacked Capacitor [below, left and right, C] more than doubles the capacitance of a conventional cell by extending its storage electrode over the neighboring cell area. Toshiba's Spread Source Drain shrinks the transistor area [bottom, left and right, D]. Each fin or storage node is encapsulated by dielectric film, which is itself encapsulated by an electrode, or capacitor plate.



C



Toshiba Corp.



D



Toshiba Corp.

is certainly the simpler. By itself, it can keep the power dissipation of 16M-bit DRAMs within acceptable limits.

However, for even greater power savings, some chip manufacturers have reduced the number of activated word lines (and therefore the number of activated bit lines) in their 16M-bit DRAMs. Such an approach is not without difficulties, however. It requires more refresh cycles, which complicates overall system design and can adversely affect chip speed.

In addition to cutting back on power consumption, lowering the bit line voltage also enhances DRAM reliability by reducing the strengths of the electric fields within the chip. As devices are scaled down and the distances between conductors get smaller, field strengths increase unless the voltage is lowered.

While on-chip circuitry will be used to lower the voltage for 16M-bit DRAMs, manufacturers have agreed to lower the external supply voltage itself from 5 V to 3.3 V for 64M-bit devices. Doing so has the obvious advantage of eliminating the need for on-chip circuitry, but it also means that there will be no 5-V bus available anywhere on the chip. Maintaining adequate chip speed with only a 3.3-V supply will not be easy, and it will be interesting to see how each manufacturer approaches the challenge.

The capacitor problem

Probably the single largest challenge facing the makers of large DRAMs is the problem of getting sufficient cell capacitance into the available cell area. Three-dimensional capacitor structures have been intensively studied for this reason. But neither the simple trench capacitor, which is a capacitor buried in a trench hole, nor the simple stacked capacitor, a configuration in which the capacitor is stacked above the transistor, can satisfy the demands imposed by the 64M-bit DRAM. Some sort of modification of one or the other will be needed.

Of the two, the stacked-capacitor approach is the more promising because it has no need for the complicated three-dimensional trench process. One modification for increasing the capacitance of a stacked capacitor, proposed by Fujitsu, is the fin structure [A in figure on p. 111]. Its storage node is formed by two polysilicon layers (the fins) and two gaps. A dielectric film covers the entire fin surface, while a cell plate of polysilicon surrounds the fins and fills in the gaps.

Mitsubishi's cylindrical cell is another method of increasing the capacitance of a stacked capacitor by increasing its height [B in figure]. Here, both the inner and outer surfaces of a cylindrical storage node are utilized as capacitor electrodes. Unfortunately, the structure's large step height makes it difficult to deposit a metallization pattern over the storage electrode.

To increase cell capacitance without an increase in cell height, a new type of capacitor cell called a Spread Stacked Capacitor (SSC) more than doubles the capacitance of a conventional cell by extending its storage electrode over the neighboring cell area [C in figure]. The storage electrode for the first cell extends over the contacts of the second and third cells. Similarly, the storage electrodes for the second and third cells extend over the first storage electrode. The result is that the storage electrodes for the second and third memory cells have a stacked structure, with the first storage electrode on the bit line contact and on the fixed oxide area. A low-resistivity plate polysilicon layer between the storage node polysilicon layers of adjacent cells shields against cross talk. The SSC cell has about twice the storage electrode area of a conventional stacked-capacitor cell.

Another way to improve the stacked-capacitor approach is to shrink the transistor area, as is done with a configuration called a Spread Source Drain (SSD) [D in figure]. In an SSD, the source-drain regions of the transistor are raised using a selective silicon growth technique. The silicon growth layers serve as buffers to prevent subsequently implanted dopants from diffusing into the substrate, resulting in a shallow source-drain junction. That shallow junction, in turn, effectively suppresses the short-channel effect and helps reduce gate length.

The shallow junction also contributes to preventing punch-through between the n-diffused layers. The benefit of that feature is reduced isolation spacing.

Moreover, the contact holes may be allowed to overlap the gates and the fields because of the lateral growth of the silicon layers over gates and fields. This is enormously important because it means that the registration tolerances of the contact holes vis-à-vis the gates and the fields are drastically reduced in the SSD transistor. The bottom line is that the total area occupied by an SSD transistor can be as little as 30 percent of that of a conventional cell.

The principal drawback of stacked-capacitor cells as a class is the large step height of their storage nodes, with its resultant difficulties for metallization. Trench-type cells yield a very flat surface because the capacitor is constructed in the trench hole. Conventional trench capacitors, unfortunately, have an inter-cell leakage current problem. For that reason, the Stacked Trench Capacitor (STC) cell, which has the stacked capacitor in the cell, has been developed and has been used in a 16M-bit DRAM.

Beyond 64M bytes

Both the trench cell and stacked-cell approaches focus the design effort on decreasing the planar area of the capacitor and optimizing its configuration. Since the transistor and the capacitor must occupy some area and are positioned next to each other, there will clearly come a point at which further down-scaling will become impractically difficult. A more innovative approach will be needed for the 256M-bit and 1G-bit DRAMs of the future.

One possible approach is a cell in which both the transistor and the capacitor lie on vertical surfaces. Such a structure is called a surrounding gate transistor (SGT). In such a cell, the capacitor is formed at the lower extremity of a pillar and the transistor at the upper end. A contact to a bit line is isolated by matrix-like trenches. The most important feature of this structure is that a transistor and a capacitor surround the side wall of a silicon pillar.

An experimental array of such cells designed under 0.7-micrometer design rules yields a cell area of just 3.6 square micrometers. In that array, the transistor gate and plate electrodes are buried entirely under the silicon surface. Thus the chip topography is quite flat and presents no metallization problems. The SGT cell realizes a small cell area, uses relaxed design rules, and is hence an extremely attractive candidate for future high-density memory cells.

To probe further

DRAM processes are covered in three major annual meetings: the IEEE International Solid-State Circuits Conference (ISSCC), the International Electron Devices Meeting (IEDM), and the Symposium on VLSI Technology.

Articles in the 1989 *Proceedings of the Symposium on VLSI Technology* include "Novel Stacked Capacitor Cell for 64Mb DRAM," by W. Wakamiya et al. of Mitsubishi Electric Corp., pp. 69–70, and "A Composed Trench Transistor Cell for 16/64Mb DRAMs" by H.P. McAdams et al. of Texas Instruments Inc., pp. 65–66. The 1990 *Proceedings* of the same conference has an article titled "A 1.28 μm^2 Bit-line Shielded Memory Cell Technology for 64Mb Drams" by Y. Kawamoto et al. of Hitachi Ltd.

The *1989 IEDM Technical Digest* includes the articles "A Surrounding Gate Transistor Cell for 64/256M-bit DRAMs" by K. Sunouchi et al. of Toshiba Corp., pp. 23–26, and "Scalability of a Trench Capacitor Cell for 64M-bit DRAM" by B.W. Shen et al. of Texas Instruments Inc., pp. 27–30.

About the author

Fujio Masuoka (A) is manager of the Device Research Department of Toshiba Corp.'s ULSI Research Center in Kawasaki. Since he joined Toshiba in 1971, he has worked on MOS LSI memories. He developed the world's first flash electrically erasable programmable ROM and NAND EEPROM. He received his B.S., M.S., and Ph.D. in electrical engineering from Tohoku University, Sendai, Japan, in 1966, 1968, and 1971, respectively. ◆

Canon: more than just cameras

Digital color copiers, laser printers, and IC wafer-steppers are among the fruits of a diversification program that began in the late sixties



Office automation is the creed today of Japan's boisterous Canon Inc. In under two decades, the company has refocused its energies, diversified its product line away from the cameras with which it made its name, and virtually re-invented itself.

Everything sprang from Canon's solid foundation in optics. Its introduction in the 1960s of the first plain-paper alternative to Xerox helped double overall sales from 1970 to 1975. This success led to a third triumph: laser printers for the PC market. Serendipity spurred a third: the bubble-jet printer.

Consequently, in addition to cameras, this major Japanese company now makes products ranging from digital color copiers to facsimile transceivers. Business machines accounted for 80 percent of Canon's consolidated sales for the first half of 1990. Of that US $5.44 billion, optical products represented only 13.7 percent and other specialties, such as semiconductor manufacturing equipment, another 6.3 percent.

Nor is there any slackening in the 53-year-old company's diversification drive. It is pushing hard to enter the computer and workstation market, despite some recent setbacks, and it is planning an all-out attack on software over the next decade.

The corporate repositioning actually began 30 years ago, but took a really radical turn in the late 1960s. Then, microfiche, electronic calculators, and office copiers were already major products, but cameras still accounted for half of sales [see chart, p. 115]. Market saturation seemed imminent, and the company small and vulnerable. Management concluded that it must diversify further.

The success of Canon's breakout from camera-product dependency, which Eastman Kodak Co. and Polaroid Corp., among others, are trying to emulate, is due in large part to the priority the company gives to R&D funding. Canon pours nearly 6 percent of its revenues from sales into R&D heavily oriented toward product development with short, two-to-three-year lead times. The company's 44 000 employees include 5000 graduate engineers, increasingly internationalized as part of a five-year Global Corporation Plan introduced in 1988.

R&D goes global

Canon now operates six research centers in Japan plus R&D subsidiaries in the United States and Europe—at Stanford and Costa Mesa, Calif., and at Guildford, Surrey, Great Britain, and Rennes, France. This year, new facilities were opened in France, Australia, and the United States, concentrating on computer research. A new research center established last spring in Kyoto is designed to attract scientists from all over the world.

All this activity has very concrete results. According to the U.S. Patent and Trademark Office, Canon has been among the top eight companies receiving patents in the six years ending 1989. It ranked first in 1987, with 847 patents granted, and third in 1988 and 1989. Yet it is not highly regarded for leading-edge technology.

Mack Chrysler Correspondent

What Canon has, said Steven Myers, a senior analyst with Jardine Fleming Securities in Tokyo, is "an ability to commercialize its core technology—high-quality optics—in a variety of areas." According to Chuck Goto, a senior analyst with S. G. Warburg Securities (Japan), who has followed the company closely for years, "Canon has refined existing technology, not introduced anything remarkable on their own. Merging microprocessors and cameras in the AE-1 and combining the key parts of a copier in a cartridge were more marketing coups than new technological concepts."

That was certainly true of the birth of the laser printer. "Technologically it was an easy improvement," *IEEE Spectrum* was told by Hajime Mitarai, 52, son of the company's founder and currently a senior managing director in charge of research and development. "You have a copier, you can use a laser beam. It is an extension of a copier. So our research center came up with a printer using copier technology. But they didn't know what to do with it."

Nowhere but up

In 1975, suffering from sluggish camera sales and an unsuccessful venture in pocket calculators, Canon paid no dividend. But that low spell proved brief. "We knew the printer was more than office equipment," Mitarai said. "We would have to go to the computer industry." Canon did so with a demonstration booth at the 1975 Computer Conference at Anaheim, Calif. IBM Corp. had also produced a laser printer but Canon's was far smaller. Hewlett-Packard Co. and Apple Computer Inc. agreed to devise the necessary computer interfaces, and Canon's goal of a new "champion product" was realized.

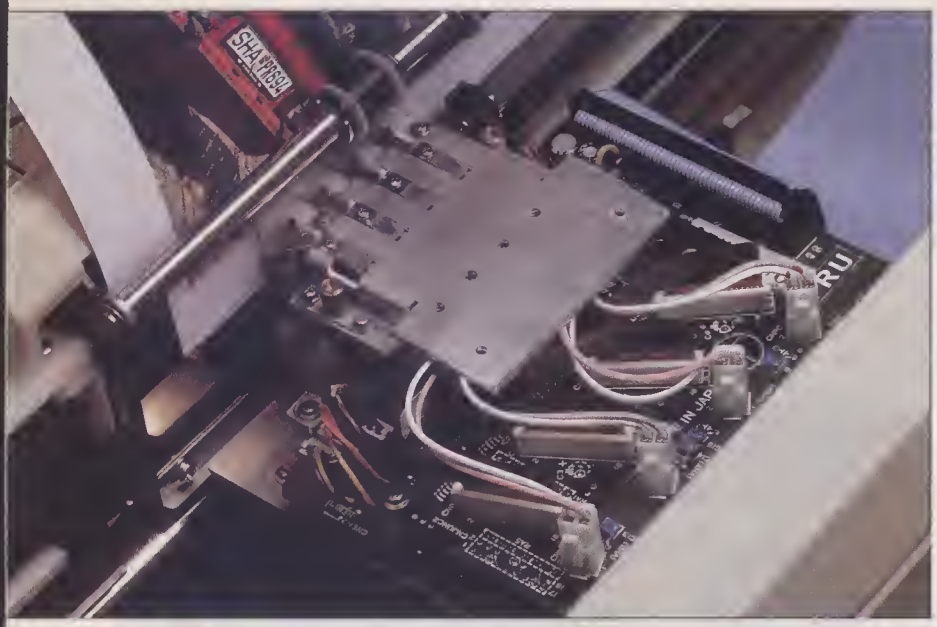
Canon replaced the bulky and costly helium neon laser in the demonstration model with a semiconductor laser, and since then, for its best-selling and least expensive model, has devised a replaceable cartridge of all the components most likely to need servicing. Today, laser beam printers underpin a new industry, desktop publishing, and although over 20 companies manufacture them, Canon supplies more than eight out of 10, almost all

Canon's switch to business machines

Year	Cameras	Business machines	Optical and other products	Consolidated net sales (millions of yen)
1970	49.1%	42.1%	8.7%	57.29
1975	50.0%	42.5%	7.6%	119.57
1980	44.0%	48.6%	7.4%	418.89
1985	20.6%	71.4%	8.0%	955.78
1989	13.1%	80.0%	6.9%	1350.91

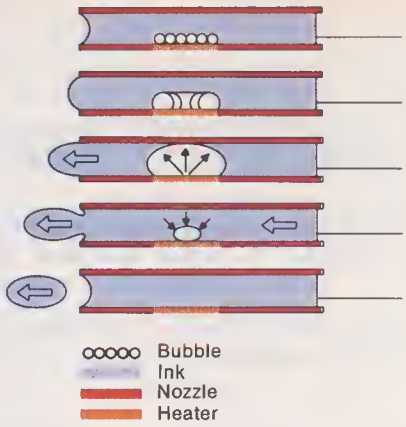
Source: Canon Inc.

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Canon Inc.



Canon's BJ-430 color bubble-jet printer has four color printheads, each with 16 nozzles to the millimeter (left, above). Instantaneous, 300 °C heat creates a bubble in the ink-filled nozzle, forcing ink out of the 30-micrometer-diameter orifice; capillary action then draws more ink in (above). Thin-film IC techniques produce nozzle arrays, electrodes, and heaters on a highly heat-conductive silicon substrate (left, below).

under Hewlett-Packard and Apple brand names.

In 1981, there was a lucky accident. One day a laboratory technician transferring ink with a hypodermic needle accidentally touched it to a soldering iron and was startled when ink squirted out. This was the origin of the printer introduced last year, which uses heat to force a bubble of ink out of capillary nozzles in the print head [see illustration].

Keizo Yamaji, now in his second year as Canon's president, predicted confidently, "Just as the laser beam replaced the daisy wheel printer, the bubble jet will replace the dot matrix printer." The bubble jet is quiet and fast, with quality almost as good as that of the laser beam. Typically, the US $499 model introduced in the United States last June was designed for broad market appeal.

But it was the 1982 debut of a US $995 copier with a disposable cartridge, incorporating drum, charger, developer, toner, and cleaner, that revitalized Canon's copy machine business. The design virtually eliminated expensive service calls and extended the copier's appeal to small businesses. Since then, Canon copier sales have multiplied more than tenfold, hitting US $3.5 billion last year and accounting for over one-quarter of the world market.

Now the company is moving into color, taking particular pride in a digital model with 400-dot-per-inch (16-dot-per-millimeter) resolution and 256 gradations available in each of four colors on every dot. According to Darrel Whitten, director of Japanese research for Prudential-Bache Securities (Japan) Ltd. of Tokyo, Canon has grabbed 70 percent of this new product market. Mitarai added that, while its copiers are currently the most profitable, "laser printers are coming up fast and within five years may pass copiers in both sales and profitability."

Phone-linked facsimile machines are another example of technological overlap: image processing, with error diffusion and edge emphasis techniques. In fax, however, Canon ranks only third among Japanese producers, behind Matsushita Graphic Communications and Ricoh Co. It is difficult for any company to achieve a significant technological edge when users seek international compatibility, and a shift to bargain marketing of low-end fax machines in Japan and the United States clouds the short-term outlook.

Longer term, as the market moves toward higher-technology facsimile equipment, Canon's future looks brighter. "Over the next few years, the key words in office automation equipment are likely to be digital and systems," said analyst Whitten, who sees new trends toward low-cost laser-based plain-paper fax machines, digital fax machines, and scanner/facsimile boards for personal computers used with laser printers or plain-paper copiers.

Shift to digital fax

The market is already shifting toward a new generation of G4 digital facsimile machines in conjunction with a more advanced integrated-services digital network (ISDN) infrastructure, which offers faster transmission and higher resolution. The bottleneck has been network availability. In this regard, the United States is ahead of Japan. But by next March 31, Nippon Telegraph & Telephone Corp. promises ISDN service to 70 percent of Japanese cities with populations over 50 000.

Canon thinks it is prepared for the fax evolution, with machines such as a plain-paper fax utilizing laser technology and a new one that can switch freely between digital and analog lines. It uses either G3 or G4 networks, but with its laser beam printing technology delivers resolution that, at 16 by 16 dots per millimeter, is four times the G4 standard and eight times the G3 standard.

Meanwhile, cameras have not been neglected. The AE-1, introduced in 1976, was billed as the world's first computerized sin-

gle lens reflex (SLR) camera. With a built-in microprocessor, it revolutionized the 35mm SLR market—in 12 years over 8.2 million were sold. One of the first point-and-shoot models followed in 1979. Within five years, Canon sold over 3.8 million Auto Boys, and 13 variations on the original theme have subsequently been marketed, with sales, still brisk, currently topping 15.5 million units.

The latest addition to Canon's camera stable is the EOS (for Electro-Optical System) 10, introduced last year. Named the 1990 European Camera of the Year, it includes three focusing sensors and a camera shake alert. The company is also conspicuous in camcorders and electronic still cameras that use photoelectric discs instead of film, but many industry observers regard its push as a defensive measure to keep up with the market shift from still to video imaging.

Another new product is an optical disc that Canon executives believe will displace floppy and hard disks for computer data storage. Their Magneto-Optical Disk is removable, offers read, write, and erase capability, and can store 256M bytes, the equivalent of 6500 pages of text, on a single side. Although Canon is not the leader in this field and competition is fierce, the Magneto-Optical Disk is installed in the new Canonfile 250. This compact desktop electronic filing system sells for 1.8 million yen in Japan and US $15 000 in the United States, including a laser printer.

Then, with 20 years of experience in producing semiconductor production equipment, the company has moved aggressively beyond mask aligners to IC wafer-steppers. In 1989, the worldwide stepper market increased 20 percent, to US $1.2 billion, and was dominated by two Japanese companies, Nikon Corp. with 46 percent and Canon with 21 percent. According to VLSI Research Inc. of San Jose, Calif., Canon is "a true threat to Nikon's No. 1 position." Lenses on current models have larger field sizes than the competition, permitting more IC patterns to be exposed simultaneously on each wafer. Last July the company introduced its new I-line steppers with a wavelength of 365 nanometers (compared with 436 nm for the g-line series), which permits more precise patterns and mass production of 16M-bit dynamic RAM chips.

Making it worldwide

If all its emphasis on product-oriented research is one reason why Canon is flourishing, then another is certainly its internationalization of production. In 1985, for example, a U.S. subsidiary was established to manufacture copiers and other office equipment. In 1986 most calculator production was moved to Taiwan. The following year a joint venture was formed with Olivetti to produce copiers in Italy, and in 1989 all electronic typewriter production was shifted to California.

According to Canon president Keizo Yamaji, the company's production in Europe and the United States has now reached satisfactory levels, and Asia is the target of new expansion. Canon currently has 13 factories as well as 35 sales offices abroad, and plans to raise the overseas share of total production from its present 20 percent to 35 percent within three to five years. It is expanding camera and lens production in Malaysia and establishing business machine factories in Thailand and China. Last year Canon recorded 30.6 percent of its consolidated sales in Japan, 30.6 percent in the United States, 31.4 percent in Europe, and 7.4 percent elsewhere.

But this internationalization has left the company susceptible to huge foreign exchange fluctuations. In two of the last five years, losses have exceeded gains by 3.79 billion yen (US $25.6 million), and a further loss of 9.11 billion yen (US $60.7 million) is forecast for 1990.

On occasion, too, Canon's aggressiveness has boomeranged. In the 1980s, for example, it was hit with anti-dumping duties on copiers and typewriters in Europe. In 1986, Aunyx Corp., of Bingham, Mass., charged Canon in a US $300 million lawsuit with trying to monopolize the U.S. market for monocomponent toner. It was decided two years later in Canon's favor but is now under appeal in a higher court. Last year, Japan's Fair Trade Commission began investigating importers' charges that a subsidiary, Canon Sales Co., was unfairly protecting the Japanese market for Apple's Macintosh computers.

The company keeps its court dates, shrugs off setbacks, and continues to bolster its product line, although in that, too, it has had failures. Canon executives still shake their heads, for example, when recalling a 1959 attempt to market the synchroreader, a machine that recorded sound magnetically on paper, enabling users to send both text and voice in a letter or memorandum. "It was technologically interesting," said Mitarai, "but such a failure in the market that our company almost went down." Another fiasco was the unsuccessful pocket calculator that lowered company fortunes in the mid-1970s. And the performance of Canon Sales in exploiting its nonexclusive rights to sell Apple computers

1937: Precision Optical Industry Co. Ltd., the forerunner of Canon Inc., is incorporated in Tokyo.

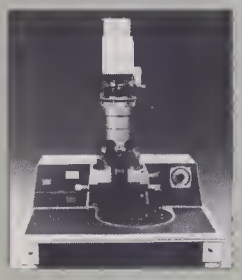
1940: The company branches out from cameras with Japan's first indirect X-ray machine.



1958: A zoom lens for television cameras incorporates optical technology from still cameras.

1959: Micrography products—microfilm and microfiche—spearhead Canon's entry into office equipment.

1964: The world's first 10-key electronic calculator is marketed.



1968: Canon introduces the first plain-paper copier alternative to xerography.

1971: The first Canon computer is marketed.

1976: The world's first computerized single lens reflex (SLR) camera, the AE-1, is put on the market, along with Canon's first facsimile transceiver.



1979: The world's first popularly priced laser printer, based on a semiconductor laser, is launched.

1982: Easy-to-maintain, replaceable-cartridge copiers go on sale, along with electronic typewriters.



1983: Canon sells its first color copier.

1985: An 8mm video camcorder and an electronic filing system are added to the product line.

1987: New products include the first EOS SLR 35mm camera, a still video camera, a 50:1 television zoom lens, and a digital color copier.

1989: Canon pays US $100 million for a one-sixth interest in the NeXT Inc. and for Asian distribution rights to the NeXT workstation.

Canon organization

Unit	Products	Global R&D
Copying Machine Business Operations	Office and personal copiers Color laser copiers Applications for copiers	**Headquarters** Future Projects Canon Research Center Component Development Information Systems Research **"E" Project Promotion Center** **Software Strategy Headquarters** **Software Business Operations** System Engineering Telecommunication Systems Development Interconnectivity Development Business Systems Market Development Corporate Intellectual Property and Legal **Product Groups' R&D Centers** Business Machines Cost Engineering Business Machines Development Trial Products Copying Machines Development Peripherals Development 1 Peripherals Development 2 Peripherals Development 3 Computer and Systems Development Desktop Publishing (DTP) and Word Processor Development Telecommunication Systems Development Micrographics Products Development Personal Information Products R&D Chemical Products Development 1 Chemical Products Development 2 Memory and Display Development Cartridge Development Photo Products Development Photo Products Project Development Still Video Camera Development Video Products Development Lens Product Technology Development Semiconductor Production Equipment Development Broadcast Equipment Development Medical Equipment Development **Research and Development Subsidiary** North America: Canon information Systems Inc. Europe: Canon Research Centre Europe Ltd.
Peripherals Operations	Laser printers Bubble-jet printers Magneto-optical disk drives/magneto-optical discs	
Business Systems Operations	Personal computers/office computers Japanese word processors/desktop publishing (DTP) Facsimile transceivers/telephone equipment/information systems	
Information Systems Operations	Micrographics products/electronic filing system Personal information products/calculators	
Chemical Products Operations	Photosensitive drums/toners Bubble-jet print heads/ink Liquid-crystal displays Copier/laser printer cartridges	
Camera Operations	Single lens reflex (SLR) and compact cameras Still video system 8MM video camcorder Lenses for SLRs/video equipment/projection TV	
Optical Products Operations	Semiconductor equipment/measuring equipment TV lenses/broadcasting equipment X-ray equipment/ophthalmological equipment/imaging equipment	
Electronic Typewriter Development and Management Center, NeXT Computer and Marketing Center, Center Audio and Visual Aids Center, others	Electronic typewriters NeXT workstation Audio and visual aids Components/product engineering equipment/others	

Source: Canon Inc.

in Japan has been so disappointingly lackluster that the U.S. company has taken complete control of Japanese marketing.

One of Canon's biggest gambles may be a controversial investment in NeXT Inc., the latest brainchild of Steve Jobs, cofounder of Apple Computer and godfather of the best-selling Macintosh. In 1989, it paid US $100 million for a one-sixth interest in NeXT and distribution rights in Asia. It wanted entry into the enticing new Japanese (and Asian) market for office and academic workstations using borrowed hardware and software. Jobs' workstation, referred to as the "black cube," is praised for its Unix 4.2 operating system, Macintosh-style user-friendly screen displays, and the 256M-byte Canon erasable optical disc. However, it is criticized for its slowness, lack of a color monitor, and limited software. Partly because of software incompatibility with both the Macintosh and IBM personal computers and their clones, the NeXT workstation has sold poorly in the United States since its introduction in 1988.

In the works

Company researchers are currently working on a new type of liquid crystal display with quick response and high resolution that could replace the cathode ray tube in computer monitors. And president Yamaji hopes that Canon is only 10 years away from producing a computer with a new operating system to rival MS-DOS and Unix.

As that aspiration implies, Canon is also addressing its shortfall in software, especially for desktop publishing and image processing in color copiers and fax machines. According to Yamaji, the company must triple the number of Canon engineers—currently 1000—in this field and get outside help, in order to catch up. Evidence of his determination is the Canon Research Center where, in contrast to the lockstep conformity typical at most Japanese workplaces, dress is casual, with blue jeans and sneakers common. "Flextime" rules the work month of 160 hours, and there are no time clocks. The researchers, mostly young men and women, are encouraged to bounce ideas off each other everywhere from the comfortable "communications plaza" to special brainstorming rooms, including one fitted Japanese style with tatami mats.

At another level, Canon managers talk philosophically—and problematically—about the need to establish more "harmony" between man, machine, and nature. Resource saving and recycling technology, they believe, will become a new business field for Canon in the 21st century.

To probe further

The Canon Story 1990/91 and Canon's 1989 annual report are both available from Canon Inc. (7-1 Nishi-shinjuku 2-chome, Shinjuku, Tokyo 163, Japan; 1 Canon Plaza, Lake Success, N.Y. 11042). Also, analyses of the company are published periodically by major securities houses.

About the author

Mack Chrysler is a freelance journalist based in Tokyo. He spent 12 years as Tokyo bureau chief for *U.S. News & World Report,* covering Japan and the Far East. ◆

The great blue box phone frauds

Until the phone company separated signaling information from the voice signal, long-distance calls could be made without charge by anyone who could whistle at 2600 hertz



Until the early 1980s, anyone who lived in the United States and could whistle in perfect pitch had a means to place long-distance telephone calls free. Those not so gifted used an electronic device almost as simple—a "blue box" that exploited a loophole in the nation's long-distance telephone network.

Blue boxes were used by many groups, each with a different agenda. The first users were mostly engineering students, who found blue boxes an inexpensive way to explore the wide-ranging phone system. As knowledge of the blue boxes became public, unscrupulous businessmen with less benign purposes, and even the youth counterculture of the 1970s, became interested in the potential possibilities of virtually unrestricted access to the U.S. long-distance network.

Although AT&T Co. conducted a vigorous campaign, both technological and legal, against blue box fraud, millions of dollars were lost in one of the costliest theft-of-service episodes in communications history. Ironically, in the end, the same forces that made the technology affordable to the toll abuser—cheap, mass production of electronic components—allowed the telephone company to eliminate the breach in its security.

Operator costs too high

Paradoxically, it was quantum improvements in phone technology that made possible frauds of this magnitude. In the early years of telephone service, operators had to manually complete all calls—both those on the same switchboard and those on distant switchboards. Foreseeing that future demand for long-distance calling would make operator service too costly, the Bell Telephone System, as it was then known, installed direct-distance dialing so that customers could complete their own long-distance calls.

As the telephone network became automated, Bell began changing to ac signaling, which operated over longer distances than the ground and polar signaling for every conversation line.

Its engineers considered three major types of signaling systems: out-of-band, external channel routing, and in-band. Out-of-band signaling transmits routing information outside the range of speech and is thus not affected by speech, echo suppression equipment, or companding—the "compressing" and "expanding" of a telephone call that takes advantage of speech information's nonuniform amplitude distribution. External channel routing transmits the routing information to and between toll centers over separate lines, removing the complexity of sorting the control signals from speech.

Both of these methods were costly, and out-of-band signaling required more sophisticated equipment to deal with the extra bandwidth. External channel routing represented an even greater installation cost, and problems occurred in coordinating calls between the signaling and voice lines.

David Flory

In-band allowed users access to the telephone network by placing routing tones in the bandwidth required for customer speech. Since they are generated by using simple oscillators, in-band tones are accepted by the routing equipment only in the absence of any other frequencies. Because speech tends to concentrate in the lower part of the voice channel bandwidth, which ranges from 300 to 3200 hertz, the phone company decided it would use as high a signaling frequency as possible: 2600 Hz.

Putting in-band into place

When Bell overhauled the trunks for the nation's long-distance telephone lines during the '50s, it selected in-band signaling because of its relatively low cost and ease of implementation. Making a call using this technology is simple. A long-distance call is first routed through a customer's local central office. Once that office has determined that the call is long distance, it locates an available long-distance trunk or tandem line, which it identifies by the idle line's constant 2600-Hz tone.

Sending a key pulse (KP) alerts the long-distance switching equipment that routing information will be required. The operator or originating automatic signaling board then sends the address digits for the number desired. The stop (ST) key signals the end of the routing information, and the call is completed.

The method of recording and charging for the call varied somewhat according to the billing area, but the charging began at the local central office when the long-distance call was answered and continued until an on-hook or hang-up signal was received by the toll office.

The widespread application of this technology required Bell to disseminate its methodology to educate its own and other telephone companies' workers. In 1954, the *Bell System Technical Journal* carried an article, titled "In-band Single Frequency Signaling," that dealt with single frequency pulsing, the first in-band signaling method installed. The libraries at most major engineering universities subscribed to the publication. That magazine's November 1960 issue became especially well known among electronics hobbyists and engineering students; in it, the phone company outlined all the signaling used for call completion, including the tones for in-band signaling.

Using a blue box

The key to using a blue box is knowing how to gain access to the long-distance switching equipment in the toll office, a procedure that was supposed to be restricted to operators and automated routing equipment. To avoid long-distance charges, blue box users first dialed long-distance directory assistance, 800 numbers (also called Inward Wide Area Telephone Service), or numbers that carried only a small toll charge. After the user dialed his number and was connected to a long-distance trunk, the blue box emitted a 2600-Hz tone, clearing the equipment at the tandem trunk's receiving end and signaling the switching equipment

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that the call had been completed and the trunk was waiting for a new call. The local central office, however, had not received its call termination signal—the phone going on-hook or hanging up—so the local central office did not disconnect the caller from the long-distance network.

Any further tones transmitted were assumed to be from legitimate Bell System equipment, so the user could reroute the call by sending new signaling tones to the interoffice tandem trunks. While all this was going on, the local central telephone office's billing equipment had not been signaled that the call had been completed, so it continued billing at the rate of the original call.

Besides allowing users to make unbilled phone calls, blue boxes provided users with access to many areas of the telephone network beyond the reach of normal customers. These included rate and route operators, test boards, conference bridges, and other internal Bell System services. Since no customer should have been able to reach AT&T employees via the restricted network, test engineers, operators, and linemen assumed that the caller was a legitimate Bell employee and freely divulged confidential information about the network.

After international operator dialing to Europe was introduced in 1963, blue box users, by virtue of their complete network access, could also direct-dial international numbers—which regular telephone customers could not do until 1970.

Blue box devices often consisted only of a tone generator necessary to produce the routing tones within the required 2 percent tolerance. Simple whistles, signal generators, electronic organs, and, later, personal computers could produce the necessary tones.

The first boxes were bigger than telephones and used vacuum tubes. By the 1970s, those using transistors, ICs, or op amps were only as large as their keypads. Some underworld crime figures made boxes disguised as cigarette packs or AM transistor radios that actually worked and could later self-destruct.

Because the correct tones were all that was needed to trick the switching equipment, many users simply recorded the tones for the number they wanted onto a cassette tape and took the tape recorder to a local telephone booth. If the user was caught during the call, no incriminating hardware would be discovered.

The chief advantage of in-band signaling—its ability to signal within the frequencies used for conversation—also helped make it vulnerable. Many eventual blue box users first discovered this loophole when they accidentally hit a 2600-Hz tone during a phone conversation by whistling.



Tony Leonardi

In the late 1960s, this phenomenon, sometimes called talk-off, increased in incidence when Quaker Oats Co. distributed whistles in Captain Crunch cereal boxes. The whistles were tuned to a high A note that was within the 2 percent tolerance of 2600 Hz. Children calling their relatives to demonstrate their new whistle were disconnected, leading their parents to complain to the Bell System, which conducted fruitless searches for broken equipment.

Enter the public

The first blue box was discovered in 1961 when a Pacific Northwest Bell business office manager noticed that the October 1961 records included several extremely long calls to directory assistance. Bell security investigated a photography studio at Washington State College in Pullman and found what they called "a strange-looking device on a blue metal chassis" attached to the studio's telephone line—hence the name "blue box."

Blue box users had a variety of motives. In the 1960s, most electronic toll fraud was committed by engineering students and the blind; estimates placed about half of the blue box users in 1968 among the sightless. Some users were more interested in finding out how the phone system worked than in cutting down on their long-distance charges. They were nicknamed "phone phreaks." For sport, some "stacked" trunk lines, routing a call through a maze of toll offices around the country and the world, adding line after line to their calls until the transmission quality began to suffer, with the call often ending up at the nearest pay phone. They then would hang up the first telephone and listen to the relays closing all around the world. The phone phreaks often adopted colorful pseudonyms such as Cheshire Catalyst, Captain Crunch, Dr. No, and Midnight Skulker.

A small but well publicized group of individuals saw the blue box as a way to further the goals of the counterculture of the 1970s. To them, it was a way to strike out at "the establishment" and to protest U.S. involvement in the Vietnam War.

As the popularity of the blue box spread, its economic potential was not lost on segments of the business community. Indeed, most fraud perpetrators caught were businessmen cutting their phone costs. Often, innocent parties discovered that they were using blue boxes installed by so-called "telephone consultants" who promised to cut the long-distance costs of their customers. Unbeknownst to their clients, these "consultants" would install blue boxes and charge clients for the long-distance service, while the calls were actually being made free.

Variations on the blue box were developed, emphasizing ease of use for those not technically skilled. Black boxes were placed on the receiving end of a call to stop the ringing before the phone was taken off-hook, preventing the phone company from being able to charge for the call.

Black boxes were especially popular with underworld criminals and bookmakers, who kept phone lines open to Las Vegas to place bets. They would use boxes to accept a call, and then automatically dial another number to reroute the call. Authorities tracing the call would raid a location only to find an empty room and back-to-back black boxes.

Red boxes simulated the sound made by a pay telephone when coins were inserted, persuading the operator that the caller had deposited the necessary amount.

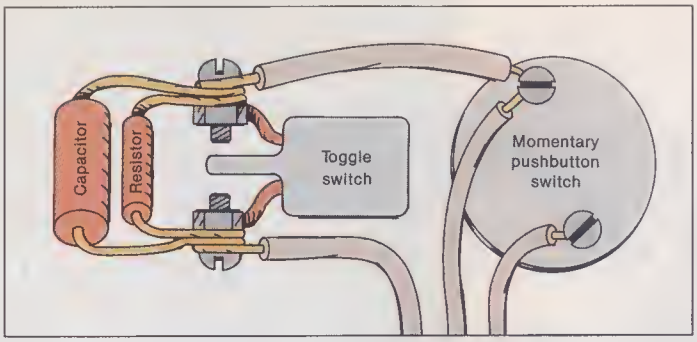
Detection technology

Faced with controlling unauthorized use of its lines, Bell first started gathering data to assess the extent of the problem. Given the size of the U.S. phone system and the relative rarity of fraudulent use, this was no small task. Between November 1965 and March 1970, AT&T operated fully automatic equipment in several cities that randomly sampled 100 outgoing trunks, five calls at

a time. When suspicious activity occurred, such as a key pulse on an active line, the call was recorded.

Of over 30 million calls scanned, 1.5 million indicated, but not necessarily proved, blue box fraud. As a result of this investigation, approximately 600 people were apprehended.

By 1970, Bell Laboratories had improved the equipment so that it recorded only the detection of 2600-Hz tones, rather than the call itself. Two years later, Bell began to regularly analyze, often with computers, central office automatic message accounting tapes for such suspicious call data as long calls to information or 800 numbers.



This illustration from the June 1972 issue of Ramparts *magazine shows how to construct a "black box," which allowed an individual to prevent the calling party from being charged for the call. The article described in simple, nontechnical terms how to ask your local electronics store for the four necessary parts (resistor, capacitor, toggle switch, and momentary pushbutton switch) and even how to identify them: "Resistor (the small part, usually brown, with the colored bands on it)."*

As Bell employees learned the ways in which the blue box was being used, they developed countermeasures. They sometimes reprogrammed local central office electronic switching system switches to disconnect a call if a pure 2600-Hz tone was detected. Because such a tone should not occur on a local switch, it meant either an equipment malfunction or fraud. Bell also countered by installing notch filters on pay phones to prevent blue box use. By 1977, the entire system was presumed to have widely installed effective detection equipment. It detected 35 boxes in New York City alone. By 1983, detection equipment was installed in virtually all heavily used long-distance circuits.

Ma Bell gets tough

Neither government nor the phone company took a romantic view of compromising the nation's long-distance network. The Federal Communications Act of 1934 mandated the Bell System to find and prosecute toll fraud perpetrators so that legitimate customers were not saddled with their costs. The Crime Act of 1968 made "fraud by wire" in connection with "access devices"—blue boxes—punishable by up to five years in prison, and/or a fine of up to US $1000.

In the mid-1960s, several states also began to enact laws against possession of blue boxes, classifying them as burglary tools, and by 1978, possession of any device to avoid payment of toll charges was illegal in at least 35 states.

In an active attempt to discourage fraud, Bell began to publicize electronic toll fraud arrests and to prosecute cases.

In 1971, 25 black box users were arrested. A year later, Bell won a court order suppressing the June 1972 issue of *Ramparts* magazine because it contained instructions for making a black box. In three days in 1972, Federal authorities arrested 14 middle- to upper-class businessmen in Chicago, Cleveland, Detroit, Houston, Memphis, Minneapolis, and other cities, confiscating 16 blue boxes. In that same operation, a Dallas company was caught selling blue boxes to businessmen for US $3000 each, advertising them as a way to cut business costs. Reports suggested that Bell security agents were investigating all kinds of fraud, even staking out telephone booths frequented by blue box users.

The end of an era

Ironically, the advances in technology that gave the phone phreak the ability to build a blue box cheaply came full circle. With the continuing miniaturization of electronic components, for example, Bell was able to design more and more sophisticated monitoring equipment to check for fraud, and stored program control switching systems allowed engineers to realize their security procedures in software—a relatively inexpensive and flexible method of searching for fraud.

The permanent solution to the blue box problem proved to be common channel interoffice signaling (CCIS)—paradoxically, a method rejected in the 1950s as too costly and difficult to implement. CCIS, instead of transmitting the signaling information along with the voice signal, puts it on a separate routing network and lines between toll centers. CCIS increases signaling capacity and versatility, reduces post-dialing delays, and eliminates talk-off. It is impervious to blue boxes because the control signaling for the network is outside the conversation band, so customers cannot reroute their own calls.

CCIS was first implemented in May 1976 between Madison, Wis., and Chicago. By 1983, the entire toll network, including 20 switching centers for the signaling messages, known as signal transfer points, were in place.

In the end, AT&T estimated the fraud to have cost between US $20 million and US $30 million each year in the early to mid-1970s. *Bell Telephone Magazine* estimated the provable loss due to blue boxes at only $1 million in 1977, but stated that the actual loss was probably around $20 million. But losses suffered were difficult to determine. Unlike those from calling-card fraud or fraudulent third-party billing, no one was falsely billed for blue box calls. Separating long legitimate calls to 800 numbers from the fraudulent ones was nearly impossible, and the stacking of telephone lines further complicated estimates.

Although some have criticized Bell for adopting a signaling system that could be so easily misused, the "Cheshire Catalyst," who formerly edited *TAP*, a newsletter that served as an information nexus for blue box users, is not one. At the time, he said, Bell had reason to believe its network was secure. The system was designed in the 1950s, and at that time, only large electronics firms like Bell had the money and skills to build the sophisticated tone-generating equipment necessary to control the long-distance trunks. Bell had no way of knowing that the technology would get so cheap that everybody would be able to use it.

To probe further

During the height of the toll fraud epidemic, hundreds of articles were written on the subject. "Beating the blue-box bandits" by Marce Elección, *IEEE Spectrum*, August, 1972, pp. 52– 58, investigated the problem of phone fraud and the legal aspects surrounding it. "Secrets of the Little Blue Box" by Ron Rosenbaum, which appeared in *Esquire*'s October 1971 issue, was one of the first widely read articles on blue box use. *Bell Telephone Magazine* published articles on toll fraud, including "Toll Fraud: Beating the Rip-Off Set," in the November-December 1972 issue, and "Fun with Dick and Jane?" by Lewis Gum and Edward Oxford in the Autumn 1978 issue.

Among the books dealing with toll fraud are *The Phone Book: What the Telephone Company Would Rather You Not Know* by J. Edward Hyde, published by the Henry Regnery Co., Chicago, 1976, and *Fighting Computer Crime* by Donn B. Parker, published by Charles Scribner's Sons, New York, 1983.

About the author

David Flory, a Cornell University graduate in electrical engineering, was selected as *IEEE Spectrum*'s 1989 editorial intern but died before he could serve. Kevin Self, *Spectrum* correspondent, assisted in posthumous updating and revising of this manuscript. ◆

The frequency that wouldn't die

North America's Niagara River is the site of operating 25-hertz hydroelectric generators that date to the dawn of the electrical age



Still generating power on the Canadian side of the Niagara River are the last operating artifacts from the birth of the electrical age. Now approaching the end of a long and distinguished career, those 25-hertz alternators gave shape to the concept of the modern electrical utility, in which generators are paralleled as necessary to meet customer demand. The Niagara Falls installation, in fact, was the world's first large polyphase central station and the proving ground for the technology now used to supply electrical power throughout the world.

In the first two decades of the 20th century, seven large hydraulic plants were built on the Niagara River. By the beginning of World War II, that area boasted the largest concentration of hydroelectric generators in North America, all of them producing 25-Hz power. Why was 25 Hz chosen for such a large block of power? Even more interesting, why has that obsolete frequency lived on for the better part of a century? The answers to such questions lie in the conditions and attitudes of the period.

When steam was king

A hundred years ago, the term "power transmission" did not connote what it does today. That was the heyday of the steam engine and mechanical power distribution. Because of their high losses, mechanical systems could transmit power over less than a few thousand meters. Many prominent technical experts, George Westinghouse among them, believed that compressed air offered the best chance for increasing transmission distances.

In 1890, it was far from obvious that electricity would provide a superior solution. The electric systems of those days were ill suited to manufacturing use. Those designed for lighting loads typically operated at 125 Hz or 133 Hz, which was not suitable for the dc motor loads of the day. Conversely, the dc systems that supplied the street railways of the era could not do so over much of a distance; there was no practical way to step up the voltage for transmission and then step it down for local use.

So when the Niagara Falls Power Company set out in the late 1880s to harness the power of the falls and distribute it in a form of use to any customer, no system of power distribution was clearly the best. Accordingly, the company directors decided to proceed without committing themselves to a particular method of distribution.

Construction of Power House No. 1 was begun by letting a contract for the turbines that convert the power of the river into mechanical energy. At least that part of the job was well understood.

Still, Edward Dean Adams, the president of the parent Cataract Construction Company, believed that electricity held the most promise, and he was proven right. In 1893 the decision was made to use polyphase alternating current as the transmission medium. By that time, work on the turbines had reached the point where their speed—250 rpm—could not be altered. That restricted the choice of generator frequency to integral multiples of 250/60. (A generator's frequency is given by its angular velocity in revolutions per second times the number of its pole pairs.) Both 16⅔ and 33⅓ Hz were proposed. Finally, a compromise was struck. The alternator would be a 12-pole machine generating 25 Hz.

But why not 50 Hz, the modern frequency for much of the world's power? Why not, for that matter, a yet higher frequency, as in the lighting systems of that era? Because the Niagara generators had a different mission: to form a central plant supplying all types of loads from a common station bus. That meant operating the alternators in parallel.

Connecting generators in parallel is a far from trivial task. The machines must be brought up to the same speed, and then their phases must be quite precisely matched before the switch is thrown to connect them. In the days before synchroscopes, the matching was done by eye, comparing the brightness of incandescent bulbs connected across the generators' terminals. The lower the frequency, the easier to make the comparison. Since throwing the switch at the wrong time could wreck a generator, ease of paralleling was a powerful argument for keeping the frequency as low as possible.

Nor was there a suitable ac motor. Before the induction motor became practical many experts believed the ac commutator motor would triumph. Since that was essentially a dc motor running on ac, it operated best when the supply frequency was as low as possible.

Why 25 Hz stuck

The 25 Hz stuck because changing frequencies is very expensive for the customer.

The major advantage of 60 Hz over 25 Hz is that it can transfer more power per kilogram of equipment. For equal ratings, 60-Hz equipment is smaller and lighter. But there was no good reason why an industry should change its existing equipment to the new frequency. So 25 and 60 Hz coexisted for many years, for as long as there was a demand for 25-Hz power, there was no incentive to convert.

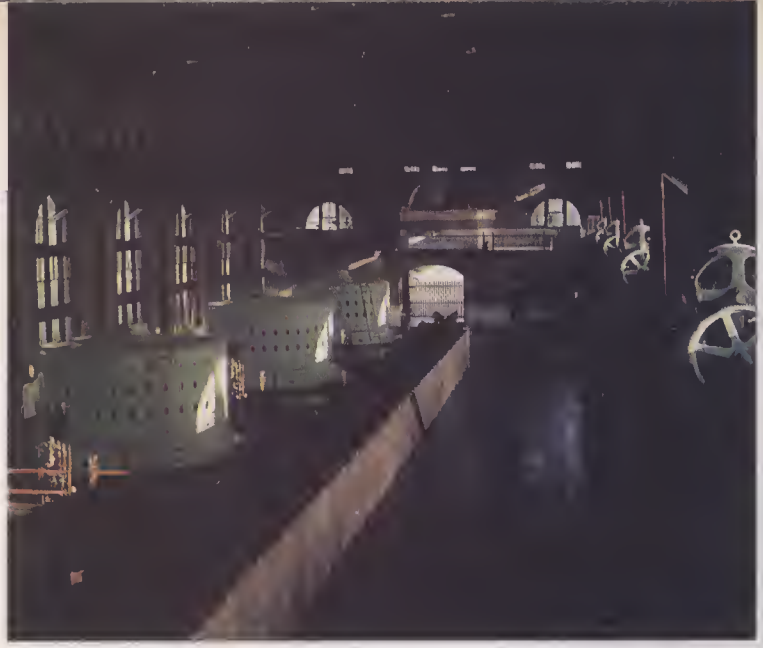
On the U.S. side of the Niagara River, traditional electrochemical industries have reduced their operations, and other industries have modernized. As a result, the requirement for 25 Hz has now almost vanished. An accident also had a major effect in the

Defining terms

Wheelpit: a deep excavation intended to house waterwheels (turbines) and associated hydraulic equipment.
Synchroscope: an electrical instrument used to indicate, by means of a pointer and a scale, the relative phase of a machine about to be connected to a station bus.

Robert D. Barnett Power City Engineering Technology

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D. Balaziak (top left), Niagara Mohawk Power Co. (below)



Canadian Niagara's original plant at Niagara Falls, Ont., is still generating 107 megavolt-amperes at 25 hertz (above). The armature of one of the original two-phase alternators is shown under construction (right). The locations of the various early installations are shown on the map.

United States. On June 7, 1956, after years of undetected erosion, the retaining wall of the Schoellkopf generating station gave way, taking with it into the Niagara Gorge the largest 25-Hz plant in the United States.

Change has been less dramatic on the Canadian side. Many of the region's original industrial operations are still there. All told, 25-Hz system capacity is about 250 megawatts.

The stations today

With the exception of the Toronto Power station, which was decommissioned in 1972, all the Canadian stations remain in operation. Two of them, Canadian Niagara's Rankine station and the decommissioned Toronto Power plant, are situated above the falls. Their turbines are located in wheelpits approximately 50 meters deep, and long shafts connect them to the generators at ground level. In that and many other respects, they are similar to the two original plants on the U.S. side of the river—Power Houses Nos. 1 and 2, the former Adams Plants.

To conceal their presence in Queen Victoria Park, the architecture of those Canadian plants is such that even a knowledgeable observer could not guess their industrial function. For esthetic reasons, even the generator power circuits were placed underground—no small task in the early 1900s.

The other two stations are at river level, in the gorge, and so are more conventional in design than the wheelpit plants. The Ontario Power plant, at the base of the falls, has horizontal-shaft generating units, an unusual arrangement today. The Sir Adam Beck No. 1, located 15 kilometers down river at Queenston, has a more modern layout: close-coupled, vertical-shaft waterwheel generators. Because of that design, six of its nine units could be, and have been, rewound for 60-Hz operation.

How long will 25 Hz last? Twenty more years might sound extreme, but so it did in 1952 when domestic conversion to 60 Hz was under way. It has lasted almost twice as long.

A new station is planned for the Queenston area of the Niagara River, and to put it on line, Ontario Hydro will begin looking to decommission the old plants to use their water rights. Converter sets will then be used to accommodate any customers who may still be clinging to the old frequency.

Seemingly, 25 Hz will not die—it'll only fade away.

To probe further

A great many in-depth technical articles may be found in contemporary issues of the *Transactions of the American Institute of Electrical Engineers* and in the *Transactions of the American Society of Mechanical Engineers*, both of which are well indexed.

As for the topic of frequency, Benjamin Lamme, the design engineer in charge of the first alternator, is the premier authority. Two of his articles in particular, "The technical story of the frequencies" in the *Transactions of the AIEE*, Jan. 18, 1918, pp. 65–89, and "The alternating current generator in America" in the *Electrical Journal*, Vol. 11, 1914, pp. 120–126, merit reading.

Two secondary sources are *Networks of Power* by Thomas P. Hughes (The Johns Hopkins University Press, Baltimore and London, 1983), which deals with the broader picture of electrification, and the two-volume *Niagara Power* by Edward Dean Adams (Niagara Falls Power Company, Niagara Falls, N.Y., 1927).

About the author

Robert D. Barnett (M), president of Power City Engineering Technology, Niagara Falls, Ont., Canada, is designing a curriculum for a course in historical technology. ◆

Global R&D for a 21st century manufacturing system

A Japanese proposal gets an initial negative reaction in the United States and Europe, but counterproposals aim at a win-win situation for all



A year ago, when Japan proposed an international research program to develop a 21st century global manufacturing system, others were not overjoyed—and some U.S. and European officials reportedly likened the idea to a Trojan horse. But now things seem to be moving forward.

The original US $1 billion, 10-year proposal was orchestrated by Hiroyuki Yoshikawa, dean of the faculty of engineering at the University of Tokyo. The intent, as stated in the proposal, was for all advanced industrialized nations to work together to find solutions to problems "that could threaten the foundation of the manufacturing industry." The proposal was offered in late 1989 by Yoshikawa to selected U.S. companies and academic institutions. It was strongly backed by the Japanese Ministry of International Trade and Industry (MITI).

Yuji Furukawa of Tokyo Metropolitan University, who had worked on the proposal with Yoshikawa, then signed up the Society of Manufacturing Engineers (SME) in Dearborn, Mich., to act as the proposal's U.S. coordinator. For the European coordination, the proposal was offered directly to the European Community (EC) as a governmental body.

When the U.S. Department of Commerce (DOC) got wind of the proposal, it complained to Japan's Embassy in Washington, D.C., that its country was making an end run around the U.S. government. And on being told that the proposal was a Japanese private industry project, DOC got into the act officially and quickly removed SME from the game plan.

"We were disappointed with Japan's approach, and the content of the proposal itself raised our concerns," was the way Mark S. Lieberman, deputy assistant secretary for technology policy at the U.S. Department of Commerce, described to *IEEE Spectrum* the department's initial reaction to the Japanese proposal. DOC's position was that MITI had bypassed the 1988 bilateral Science and Technology Agreement with the United States and was designing the program to gain access to U.S. software, artificial intelligence, and system integration technology without providing an equitable exchange of Japanese technologies.

Reaction of the EC was even stronger, Lieberman told us in his Washington office. "They were even more skeptical," he said.

Shortly afterward, representatives from the DOC and the EC met to compare reactions to the Japanese proposal and to set a course of action. As a result, both organizations are now offering counterproposals, and Japan has revised its proposal to take at least some of the U.S. and EC concerns into account. A meeting scheduled in Japan, November 19–20, will attempt to begin to resolve differences to the satisfaction of all three parties.

Late 1989—Japan submits its proposal

The original proposal for joint international research programs to develop an Intelligent Manufacturing System cited Japan's expertise in production management and in developing factory automation units such as computer numerically controlled machinery and industrial robots. It also noted that the United States was well versed in software and network technology and that Europe was strong in complex precision machinery. "By fusing the various technological advantages of Europe, North America, and Japan," the proposal stated, "it is possible to develop, in a most efficient manner, innovative production technology which meets the unique demands of the coming century."

The US $1 billion funding for the 10-year program called for the Japanese Government to supply US $400 million; Japanese industry, US $200 million; European governments and industries, US $200 million; and the U.S. government and corporations, US $200 million. The proposal also stated that a joint international research center would be set up in North America and/or Europe.

The R&D domain of the program [see illustration] encompasses the entire range of production technology from basic technology to potential commercialization.

Examples of R&D topics aimed at the 21st century manufacturing system were outlined in the proposal, together with the approximate time for peak activity during the life of the 10-year program [see table].

April 1990—DOC takes over

In an April meeting of U.S. industry and academia representatives at the National Institute of Standards and Technology in Washington, D.C., the participants suggested that the U.S. government take a leadership role in negotiating for a more equitable program.

DOC responded by raising the issue at a high-level meeting attended by representatives of the U.S.-Japan Science and Technology Agreement. There it was determined that the Japanese proposal would be put under the jurisdiction of the agreement's section on advanced manufacturing.

May 1990—Trilateral meeting in Brussels

The next step was a convening of a trilateral May meeting in Brussels, Belgium, where the United States, the EC, and Japan agreed that:

- Any intelligent manufacturing system (IMS) proposal would be coordinated and communicated by the appropriate Governmental offices of each community.
- Any proper collaboration must have a balanced flow of knowledge.
- Before there is any IMS program, agreement must be reached by all three on modalities of cooperation, technical content, intellectual property rights, and funding arrangements.
- A jointly prepared program for cooperation is a must.
- Each side will conduct extensive consultation with its industry and academia representatives to develop a rational position.
- In particular, Japan agreed to: supply DOC with all past

Ronald K. Jurgen Senior Editor

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proposals; stop soliciting proposals from the United States and the EC; defer all U.S. inquiries to DOC; and make all communications with U.S. companies through DOC.

July 1990—DOC's counterproposal

In July, DOC convened a meeting with representatives of U.S. trade associations and academia to explore questions arising from the Japanese IMS proposal and determine what the U.S. position concerning it should be.

Using inputs gathered at that meeting, DOC prepared a draft "strawman" U.S. proposal for international collaboration on advanced manufacturing systems. Guidelines are:

- The three entities would have equal voting rights.
- Each party would decide how its financial and other contributions should be structured, including the percent of industry and government participation, access to research facilities, unique expertise, and so forth.
- Technical projects would consist of tripartite consortia with at least one industry participant from each tripartite member. Bipartite consortia would be acceptable subject to tripartite approval.
- Funds from the program would not go for the construction of research centers, structures, or laboratories.
- Multilateral participation in the projects would be encouraged.

Specified areas in which the United States could benefit from such an international collaboration are:

- International standards for advanced manufacturing and information technology.
- Techniques for rapid commercialization of R&D results.
- Information technology such as advanced database structures and techniques for manipulating large-scale distributed knowledge bases.
- Enterprise integration techniques for integrating the technology and business elements of a manufacturing enterprise.
- Precision engineering.
- Intelligence control technologies.
- Quality engineering and management techniques.
- The application of intelligent control technology to the manufacture of high-quality, precision-engineered, mechanical-electrical products such as videocassette recorders and step-and-repeat cameras.
- Market identification and development.
- Process technologies such as for metals and semiconductors.

Concerning intellectual property rights, it was suggested that the guiding principle should be that participants have equitable control of these rights, taking into account their investment of resources to the program, including facilities and unique expertise as well as direct funds.

Topics on intellectual property rights selected for further dis-

R&D topics in the original Japanese intelligent manufacturing system proposal

Production system development technologies for:

- Autonomous and decentralized production
- Interfaces (design and production)
- Variable and flexible production
- Small-batch production
- Production control using artificial intelligence (AI)
- Quality control using AI
- Facilities renewal using AI
- Supporting intelligent computer-aided design
- Manufacturing systems (autonomous and decentralized scheduling)
- Evaluating production systems
- On-line inspection

Production-related information and communications technologies for:

- Manufacturing systems (real-time decentralized)
- Setting up and controlling knowledge bases for manufacturing systems
- Integrating production databases
- Production simulation
- Production control and management using fuzzy logic
- Production control and management using neuro-logic
- Automatic preparation of manufacturing documents
- Inputting three-dimensional information
- Manufacturing equipment (remote-control)
- Real-time image processing for manufacturing systems
- Standardization of product models
- Standardization of regulating networks
- Standardization of electronic transactions
- Standardization of conversational graphics
- Interfaces for cell-based communications
- Application of interfaces to manufacturing system networks
- Using overseas networks through satellites

Production-control equipment and processing technologies for:

- Three-dimensional recognition
- Production-control using expert systems
- Fault tolerance for manufacturing systems
- In-process sensing
- Autonomous robots
- Skill-replacing robots
- Scheduling for cooperative robots
- Sophisticated autonomous functions in numerically controlled systems
- Energy beam processing
- Multifunction integrated processing
- Autonomous decision-making in automatically guided vehicles
- Direct numerical control for automatically guided vehicles
- Using automatically guided vehicles in clean rooms
- Automatic inspection using AI
- Imparting sophisticated functions to automated warehouses

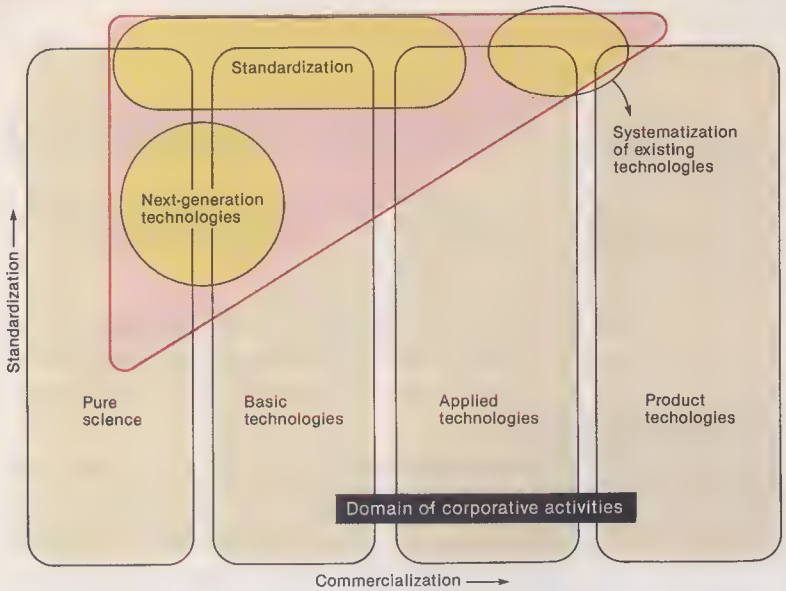
Application technologies for new materials involving:

- Ultra-heat-resistant ceramics and composite metals
- Ultrahigh-strength and tough materials
- Function-oriented composite materials
- New sensors
- High-capacity batteries
- Materials handling
- Advanced structure analysis
- Products made from soft materials
- Solid image sensors
- Holograms
- Infrared camera devices

Human factors in production, encompassing:

- Research into the area as a whole
- Research into human factors in architecture
- Research into the role of humans in sophisticated automated plants
- Technology for optimizing the production environment
- Human mimetic technology
- Measuring technology using human-like senses
- The use of multiple media at the human interface
- The use of inferential and learning capabilities in man-machine interfaces
- On-line consultant technology
- Computer-aided instruction for manufacturing systems using expert systems
- Artificial reality technology in production

● Early period ● Middle period ● Late period



Domains of research spelled out in the original Japanese proposal for an intelligent manufacturing system are shown in the triangular color area at the top.

cussion include: the rights will be assigned in accord with the U.S. Government Intellectual Property Rights Annex for international agreements; such rights in Third World countries should be determined by mutual agreement of the parties; U.S. participants shall have the sole power to decide issues such as royalty rates, sublicensing rights, and so forth within the United States; and software developed in the course of research will be treated consistently with these recommendations.

Several questions were raised concerning the contributions to be made to cooperative projects:

- How will each partner assess the weight of its potential contribution in unique research facilities, expertise, and other noncash resources?
- Should there be a centralized funding pool set up for all projects, modeled after the National Science Foundation paradigm?
- Should industrial contributors be allowed to target funds to specific research areas?
- Should a specific mix of private sector and Government funding be required?
- Should current domestic efforts be accounted for, and as appropriate reformed to provide a partner's contribution (in-kind matches from existing programs like Esprit, Brite, and Mantech)?
- Should reprogramming existing R&D funds be targeted in lieu of seeking new funds?
- What should be the relationship, if any, between the overall contribution provided by an industrial participant, including funding families and expertise, and the control of the project agenda and the distribution of benefits?

July 1990—EC's counterproposal

Later in July, the EC described to DOC officials an outline of their counterproposal calling for the program to be renamed "Future Generations Manufacturing Systems." It cited as the key issue the modalilities of cooperation and said that other issues were dependent on that issue's being resolved. It also stated that there would be no research centers but a regionally distributed work program made up of tripartite working groups instead.

With regard to proposals, the EC said there would be a call for them to the members, they would be made by tripartite consortia, and they would all require tripartite evaluation and approval. In addition, each region would fund corresponding subprojects, bipartite consortia could be acceptable in some cases but subject to tripartite approval, and the composition of consortia could be modified only by tripartite agreement.

The EC also recommended that the first year focus on a feasibility study of technical areas and that it include a pilot project.

Additional recommendations on intellectual property and exploitation rights include:

- Intellectual property shall be owned by the participants generating the information involved.
- Summary information shall be made available to all participants in the program.
- Participants in a project shall have royalty-free rights to the intellectual property emanating from the specific project for use in that project.
- Participants in the same subprogram shall be granted limited rights to the intellectual property at cost.
- Participants in the program shall be granted limited rights to the intellectual property at the market rate.
- All participants in a project who have made a significant contribution to the project shall have free full rights to the intellectual property originating from the project.
- All participants in a project shall grant each other full rights in any software resulting from the project, including the right to sublicense in the normal course of their business.

August 1990—Japan's counterproposal

In August, MITI submitted a revised intelligent manufacturing system proposal to DOC. It suggested setting up a trilateral government meeting to establish basic principles, a steering committee made up of world authorities from industry and academia, and both a technical committee and an intellectual property rights committee to advise the steering committee.

The Japanese proposed action in two stages. First, companies, universities, and research institutes from each region would form consortia; existing international research centers would be used; and members of each consortia would pursue research jointly by networking together and exchanging information. Also, secretariats would be formed as necessary, and governments would provide subsidies at their discretion.

In the second stage, a joint international research center would be established in one of the three regions; each region would fund one-third of research with the ratio of funding in each region individually determined; and each region would convene a meeting of experts to consider R&D topics to propose.

In the Japanese counterproposal, ownership of the rights to research results would be determined according to the degree of contribution of each researcher. Registration and protection of rights would be handled according to the nature of the rights involved and the laws that consequently apply. Participants in the program would be given priority access to the results as soon as possible; the general public, at the appropriate time.

September 1990—DOC workshop

On Sept. 26, DOC held a workshop in Washington, D.C., at which the status of the intelligent manufacturing systems project was presented. Participants were presented with questions about the DOC strawman proposal. The inputs from the workshop will be used by DOC to develop its proposal, which will then be discussed in Japan in November.

Those discussions will have significance beyond simply the success or failure of the intelligent manufacturing system proposal. If the program can be structured to the satisfaction of all parties, it will pave the way for future such initiatives from Japan.

Phyllis A. Genther, director of the Japan Technology Program at DOC, told *Spectrum* that MITI already has other specific proposals in mind. But Hidehiko Nishiyama, deputy director of MITI's Industrial Machinery Division, told us that no decision has yet been made on any future proposals. ◆

Whatever happened to?

The paperless office

Each day, U.S. companies produce about one billion pieces of paper. This is broken down into 600 million equivalent pages of computer printouts, 234 million photocopies, and roughly 100 million copies of other paper documents.—"Information and Image Management: The Industry and the Technologies," Coopers and Lybrand, Association for Information Management, Silver Spring, Md., 1987.

Evolving technologies such as magnetic and optical storage, electronic and voice mail, and video systems were supposed to rid the office of paper documents. Yet paper usage still grows by nearly 5 percent per year, and the paperless office remains a myth.

There are several reasons why paper does not vanish. First and foremost, it is still people's preferred way of absorbing complex information, thanks to their training, history, and culture. Schools still focus on the printed page even though electronic alternatives are gaining. Books, newspapers, and magazines are still the principal media throughout the world for presenting information.

Second, the very products that 15 years ago promised to pension off paper—the personal workstation and the desktop computer—are instead promoting its use. With word-processing software, complex documents can be produced efficiently—business graphics and scanned photographs as well as more complex images.

More to the point, almost every workstation and personal computer has a printer connected to it. And to further encourage the use of paper, modern printers—particularly laser and ink-jet types with gray-scale capability—can create documents out of a multitude of fonts, graphs, and images. Furthermore, color ink-jet printers and, to a lesser extent, color thermal transfer and color laser xerographic printers are on the scene.

Third, modern copiers, whose products often look better than the originals, produce more than 100 pages per minute. That capability encourages a wider distribution of all documents, but especially those with many pages.

Finally, the use of office and personal facsimile equipment has ballooned, and the thermal-paper facsimile messages are often copied onto plain paper and the originals discarded.

Such innovative products readily conjure up image-rich documents that can be circulated far and wide. When workstations and printers are networked, documents generated in one location can be printed in another, further multiplying the number of complex documents that are consistently printed before they are even read and found to be worth printing.

Increasingly, documents will be generated electronically, communicated electronically, and filed in electronic form. Image scanners will allow bitmap recognition of text. The ability to parse complex documents into text and graphics will improve the efficiency of transmission and storage of electronic documents.

Few people enjoy studying a document in electronic form if it is long or complex, requires browsing or rereading, or needs to be transported or annotated. Only when the message fits into one page do most people care to review it on-screen.

To induce people to work with electronic documents, four technological advances are needed: personal software filters, better flat-panel displays, browsing algorithms, and the ability to annotate documents electronically.



Tony Leonardi

Personal software filters that can be adjusted to one's daily needs would make a big difference. For personal use, systems available today for doing library and database searches are too compute-intensive and expensive, and come with dauntingly complex user interfaces. There is also a need for filters of incoming information, which individuals can set daily or even hourly to recover only what they need.

Such information filters should be front-end additions to personal workstations, private files, and fax machines and should be adjustable for key words or phrases. They should rate incoming information on the basis of user interest. In the long term, they should learn the characteristics and preferences of the individual user.

Another necessity is a method for acquiring information that will not be needed until later. Robert Kahn of the National Research Initiatives Corp., in the May 1990 issue of *Science*, envisioned a personal software knowledge robot—he called it a personal knowbot—that could be sent out to public and private databases to collect information required for a particular task and transmit it in capsule form to the user. The knowbot could also contact key individuals within or outside one's company for their opinions and input. For knowbots to be used extensively, large public and private databases would have to be connected by wideband, high-speed networks.

Before people will use electronic information more heavily, better flat-panel displays are necessary. High-resolution displays, with color that could eliminate glare and operate in any light, would greatly enhance the comprehensibility of electronic information. The displays would, of course, have to be low-power, lightweight, inexpensive devices.

Today's laptop computers have enough memory to store documents, but need to be lighter in weight and consume less power. Since both displays and memory depend on silicon IC technology, however, weight, power, and size should continue to halve every three years.

And to further undercut the popularity of paper, it will be necessary to develop both improved browsing algorithms for complex documents in electronic form and the ability to annotate documents electronically. One reason facsimile has such appeal is that the user can annotate a document almost anywhere and transmit those annotations immediately. That, coupled with the ease of identification of sender and receiver through the telephone system, has fueled the explosion in the use of facsimile. If personal workstations had a similar capability, electronic documents would find a much warmer welcome.

As computational prowess and software developmerit zero in harder on information needs, the trend will be away from strictly paper information and toward information in electronic form. But to assimilate information in the foreseeable future, most people will favor paper.

William J. Spencer Sematech Inc.

About the author

William J. Spencer (F) became president and chief executive officer of Sematech Inc., Austin, Texas, Nov. 1. He had been group vice president and senior technical officer, Corporate Research Group, for Xerox Corp. in Stamford, Conn., since 1986. Previously, he had been vice president and manager of the company's Palo Alto Research Center. ◆

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Japan telecommunications at the crossroads

In 1985, Japan introduced competition into analog communications, but now digital technology has changed the industry—so what should be done?



In 1985, with Japan's enactment of the New Telecommunications Business Law, the Japanese company Nippon Telegraph & Telephone Public Corp. was turned from a Government-owned monopoly to a private company, Nippon Telegraph & Telephone Corp. (NTT). The new law aimed to introduce competition and reduce charges in toll (long-distance) communications and to diversify services, while maintaining low-cost universal local service and NTT's technological capability.

In the past half decade, however, toll charges have remained higher than the international standard, competitors have not been as successful as desired in providing new services different from those offered by NTT, and labor productivity has been modest compared with other Japanese industries. In addition, the 1985 law is now facing complaints from new common carriers, which are calling for a completely revamped policy.

Part of the reason for this outcome has been advances in technology itself: the advent of the integrated services digital network (ISDN). When NTT was privatized, analog communications were well established and dominant in Japan. But ISDN, now being introduced into NTT's network, is upsetting market conditions for businesses based on analog technology, posing political and economic problems not anticipated in 1985.

The 1985 law included an article requiring a review of the structure of the Japanese telecommunications industry after five years. This March, the country's Telecommunications Council of the Ministry of Post and Telecommunication of Japan (MPT is Japan's counterpart to the U.S. Federal Communications Commission) published a report suggesting that NTT actually be split up into one local telephone company and one toll company. This breakup would be analogous to the way the U.S. Bell System was split up into seven local companies and one toll company in 1984, and for similar reasons: to solve the problems of unequal competitive conditions existing between new common carriers and a single dominant carrier.

Although this year any decision to divide NTT was tabled until 1995—a political move made because of NTT's low stock price—many experts feel some major step is necessary. A simple breakup may not help solve the problems in the industry, but continuation of present regulation will only make them worse.

What should be done?

Intent versus result

When NTT was privatized, the major areas into which competition was introduced were long-line transmission, cellular services, value-added network (VAN) services, and customer-premises equipment. To minimize the impact of this change on NTT's business activities and technological capabilities, the company itself was not required to change its overall corporate structure. It was believed that telecommunications in Japan could be diversified and costs driven down by introducing competition while still maintaining the stability and universal service of a monopolistic system. In this key respect, the NTT privatization differed from AT&T's divestiture a year earlier. In fact, it is more akin to the U.S. situation in the early 1980s right before the divestiture, when the FCC was trying to introduce regulated competion against the Bell System.

Unlike the case in the United States, basic communications service (transmission and switching only) in Japan was not distinguished from enhanced communications services (requiring some information processing). Instead, the major distinction was ownership of transmission facilities.

NTT and those few toll carriers that do own their own transmission facilities were designated Type 1 common carriers; most VAN providers, which lease transmission facilties from the Type 1 common carriers and then customize them to offer other services (such as digital data) were designated Type 2 carriers. In addition, some Type 1 common carriers, including NTT, also offer VAN services. Type 2 carriers are categorized as special (those with more than 500 circuits) and general (those with fewer than 500 circuits). The Ministry of Post and Telecommunication (MPT) regulates services, tariffs, regions of operation, and so on of only the Type 1 carriers. Type 2 carriers operate essentially without regulation.

Overall, experts agree that the privatization of communications in Japan has successfully expanded competition. In the last five years, the number of NTT's competitors has gone up by an order of magnitude—many more than initially expected [see Table].

Over that same five-year period, with the advent of the competing long-distance carriers, the charge for long-distance calls has also dropped by 30–50 percent [see figure on the opposite page]. But by international standards, the charge for a long-distance call in Japan is still much higher than that of other countries. Users have been frustrated with the situation, but it is difficult to motivate the other Type 1 common carriers to reduce their toll charges drastically, and they tend to fix their charges

Defining terms

Type 1 common carrier: a common carrier that owns transmission lines and can provide both basic and value-added communications services.
Type 2 common carrier: a common carrier that does not own transmission lines, but leases them from Type 1 carriers. These carriers offer only value-added services: they are classified into Special Type 2, which have more than 500 circuits in their networks, and General Type 2, which have fewer than 500 circuits.
Value-added network (VAN) service: a service that is resold by providing basic communications plus an added feature, such as a leased line with packet switching.

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at a level a little cheaper than that of NTT. Since the rates are decided based on a petition from each carrier, the MPT cannot set the actual rates.

Even more seriously, NTT's labor costs have still remained higher and productivity lower than those of other Japanese industries. For example, in 1987 NTT's labor cost as a percentage of total costs was about 36 percent, while the average percentage in service industries overall was 15 percent and in large-scale retail industries, about 10 percent. One of the reasons is the strong influence of labor unions on NTT's management, and neither the unions nor management has worked very hard to improve labor efficiency. To be fair, relatively high labor costs in communications companies is a common problem worldwide—it is not unique to NTT. But it does mean the privatization of NTT did not achieve one of its principal ends of substantially lowering costs in a short time.

One-way flow

It was once considered difficult to reach quick profitability in the communications industry since a great deal of initial investment is required. However, although figures vary for companies in the industry, many are enjoying steady growth. All three Type 1 common carriers providing toll communications service (Daini Denden Inc. or DDI, Japan Telecom Co., and Teleway Japan Corp., all based in Tokyo) reported a profit in fiscal year 1989 (which ended in March 1990).

New Type 1 firms are also entering local and regional communications. But here NTT has a considerable advantage. The local infrastructure, which includes the subscriber distribution system that was built during the monopoly period, helps NTT keep local telecommunication rates low. New Type 1 carriers must construct their own distribution systems, requiring a tremendous investment over a short time. Since the local-distribution technology is mature, significant cost reductions characteristic of new technologies cannot be expected. Therefore, local distribution services do not yield profit to the new firms joining the field, and the number of local networks competing with NTT is limited. The only exception is some new firms handling cellular radio and paging services.

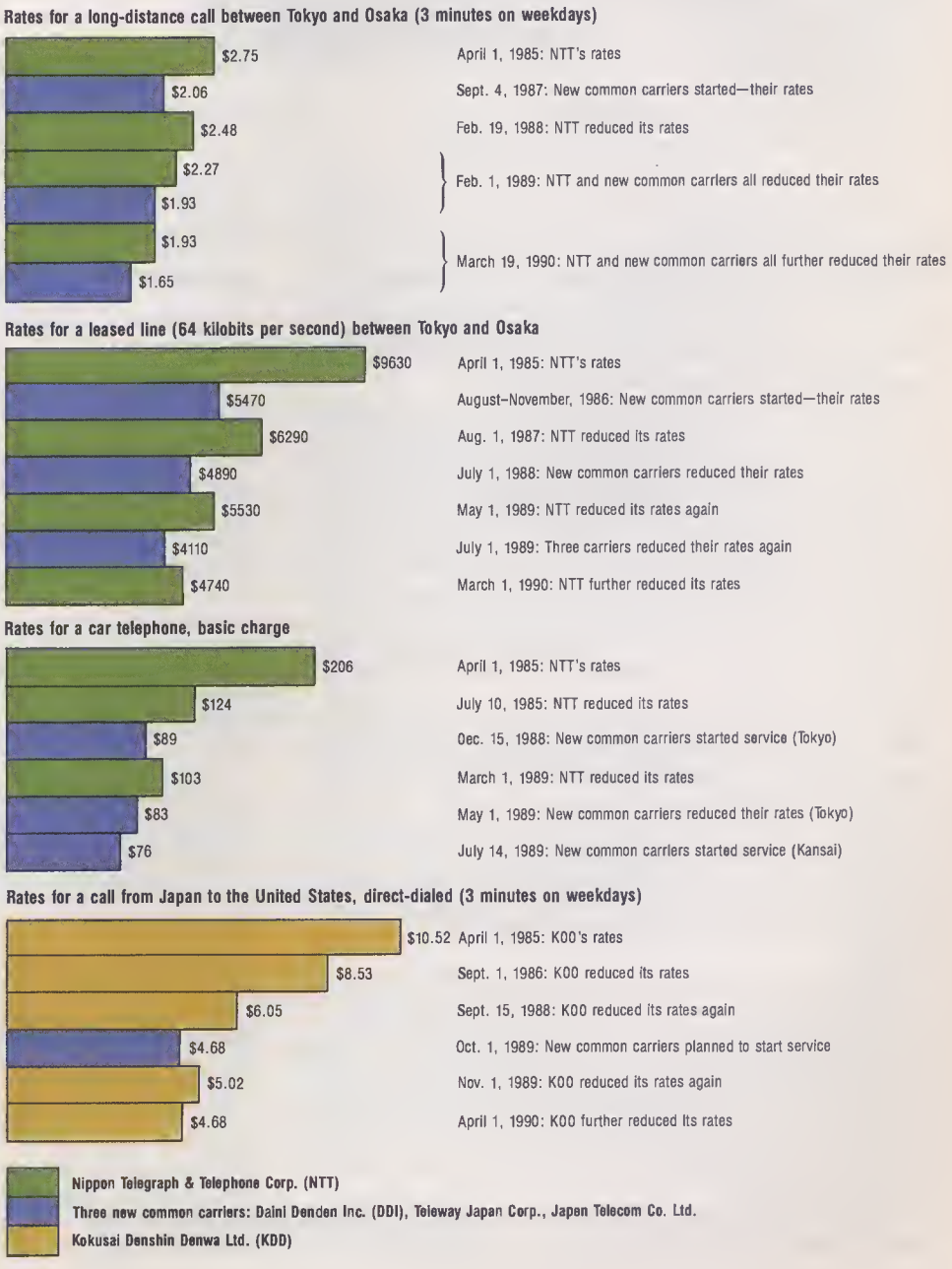
For these reasons, the Japanese communications network depends principally on NTT for local service. Local and long-distance carriers alike are becoming increasingly aware that the demand for their services depends on NTT's support—and that, indeed, they cannot continue in business without the good will of NTT, their competitor. They cite three principal problems.

First, NTT has significant control over the market because it possesses technology and the R&D capabilities accumulated during its monopolistic years, and it is overwhelmingly larger than that of any other carrier. DDI—the largest new common carrier—has an annual revenue of 100 billion yen (about US $700 million), which is less than 2 percent that of NTT.

Second, NTT cross-subsidizes its various services, so that the revenues and expenditures of each type of service—local and toll call charge—remain unknown to non-NTT carriers. Third, NTT automatically obtains much information (such as the amount of business traffic in one particular region) about new common carriers through their connection with the local network, but those carriers cannot in turn obtain similar information about NTT. In addition, in many cases, NTT unilaterally specifies interfacing requirements, discouraging innovation by the other common carriers. Although these problems can be mitigated by the good will of NTT, they nonetheless all add up to unfair competition.

As a result, many of the new common carriers now want NTT to separate the local network from all other NTT services; this would be analogous to the AT&T divestiture, in which local ser-

Reduction of rates—a major objective of the privatization of Nippon Telegraph & Telephone Corp. and the introduction of competition into the telecommunications industry—has been at least partially successful.



vice was given to the seven regional holding companies that are operated as regulated monopolies, allowing all interexchange carriers equal access to the local network. Such a separation, many Japanese experts believe, would give the new common carriers equal access to the local network.

Fears for the future

Some experts fear that splitting up NTT could adversely affect low charges for local calls, original communications technology, and reliable management of a unified network.

It has been suggested that Japan adopt the U.S. model of keeping local rates down by having toll companies pay an access charge for connecting with the network. But in the United States, the access charge consumes nearly half the sales of the toll companies, leading some to question how long the new—and relatively small—toll carriers in Japan could bear such a burden. Right now NTT is the only carrier that, in effect, pays access charges, as its long-line business section cross-subsidizes its local services. Other common carriers are completely exempted from paying access charges—and even the 1990 Telecommunication Council proposal to split NTT maintains that exemption.

Number of new common carrier companies in Japan after Nippon Telegraph & Telephone's privatization

Fiscal year[1]	1985	1986	1987	1988	1989	1990
Type 1 common carriers[2]	0	5	11	35	43	62
Type 2 common carriers (total)[3]	85	209	356	530	693	841
General Type 2 common carriers[4]	85	200	346	512	668	813
Special Type 2 common carriers[5]	0	9	10	18	25	28
Total new common carriers	85	214	367	565	736	903

1 Beginning April 1 of each year.
2 Type 1 common carriers own their own transmission facilities.
3 Type 2 common carriers lease facilities from Type 1 carriers.
4 General Type 2 common carriers have fewer than 500 circuits in their networks.
5 Special Type 2 common carriers have more than 500 circuits in their networks.

Although NTT's research and development is recognized as a great contribution to Japanese technological capabilities, others question whether a split would prohibit the central company from continuing the same level of technological effort. Such a research organization, if lost, would require much time and effort to rebuild, and any negative impact is likely to be long lasting. In the 1990 report, MPT's Telecommunication Council advised that if NTT were divided into one local service company and one toll company, the laboratory should remain a part of the local service company. It also urged that the local service company keep a majority of the present revenue of NTT, allowing it to support the necessary R&D.

Between 1985 and 1990, however, the stock price of NTT has fallen. When NTT was privatized, the Japanese Government successfully obtained a substantial amount of money by selling NTT stock. At first, each share sold for about 1.2 million yen (about US $8000) and boomed to more than 3 million yen (about US $20 000). But with a 1988 scandal in which NTT president Hisashi Shinto was accused (and later convicted) of taking bribes from the Recruit publishing group in Japan, followed by a general slump of the Japanese stock markets in 1990, NTT's stock price dropped.

Japan's Ministry of Finance, fearful that NTT's stock price fall might accelerate with the decision to break up the company, opposed the Telecommunication Council's 1990 report. Because of that opposition, the Japanese cabinet postponed the discussion of a breakup for another five years. In spite of this decision, NTT's stock has continued to fall, along with the stock market in general. In September 1990, NTT's stock price was lowered to 700 000 yen (about $5000). Only time will reveal if—and how well—it will recover.

The shift from the analog system to ISDN in Japan's communications network is not merely a technological change. It is causing complicated shifts in the whole competitive structure of communications.

For example, there is the situation that occurred with packet switching after ISDN was introduced. Traditionally, packet switching, supplied to fewer users than telephone services, was provided by NTT and a few special Type 2 common carriers as a digital service separate from the conventional analog network. Before the advent of ISDN, a single packet-switching access node was established in each city, and a subscriber's line was installed as a leased circuit between the subscriber's premises and the access node. Such a line was often longer than 10 kilometers, and most of the monthly charge for the service (generally about 20 000 yen or US $140) reflected the cost of laying the line. A similar basic cost applied to both NTT and the special Type 2 common carriers.

With ISDN, however, all central office switches provide both circuit switching for conventional telephones plus packet switching, which allows all telephone exchanges in a city to have the packet-switching function. The subscriber's line need run only to the nearest central office. As a result, the line charge for packet switching over ISDN is much lower than that of the conventional packet-switching service—leaving the Type 2 common carriers totally uncompetitive with NTT's ISDN.

After negotiation with NTT and MPT, Type 2 carriers have been allowed to use the ISDN local access facilities to offer their services. Originally, ISDN was conceived as one complete integrated network. However, if a number of Type 2 carriers use only a fraction of available ISDN lines and also add various technologies for VAN services, maintaining network integrity could be formidable.

The main problem

These changes in Japan's communications industry spurred by technology have created many conflicts within the country's communications network since the privatization of NTT. It cannot be denied, though, that such problems arose in part because of the major premise underlying the 1985 change: to retain the advantages of a monopolistic network even in a competitive arena. To resolve such antagonisms, possible next steps—including the division of NTT—are being discussed, and the Telecommunication Council is studying the structure set up by the AT&T divestiture.

Some Japanese experts—including myself—feel that the answer is not to support old technology past its time, but to devise a new structure for regulation fitted to the circumstances created by the new technology. New technology cannot work properly if it is not accompanied by a correspondingly new industrial structure.

Whatever happens, however, the experience of 1985 shows one basic lesson: to be successful over the long term, such discussions must focus not just on existing service suppliers but on future technological development and on the appropriate corresponding form for the network.

To probe further

This article is a translation and condensation of the author's six-page special report, "Fifth Anniversary of Telecommunication Regulation," published in the Japanese edition of *IEEE Spectrum* by Maruzen Co., Tokyo, vol. 3, no. 6, June 1990.

About the author

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Applicants should have a Bachelor's degree in Engineering, a related science, or the equivalent; 5 or more years' related background, at least 2 of which are in operations (must be in I&C/process control for one of the openings); and 2 years of engineering experience. Power plant experience is preferred. The chosen candidate will be expected to travel about 40% of the time.

We offer excellent salaries based on experience and benefits including medical, dental and vision, an employee savings plan as well as 4 weeks' vacation and 13 paid holidays. To apply, please fax or send your resume and salary requirement, in confidence, to: Employment Administrator, Dept. AT, New York Power Authority, 123 Main Street, White Plains, NY 10601. Fax: (914) 287-3228. An affirmative action/equal opportunity employer.

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- Design CAD tools to support simulation, layout, circuit design, high level modeling and layout verification. Experience in CMOS VLSI design required.

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For immediate consideration, please send your resume to: **Intel Corporation, Dept. S168, P.O. Box 58121, Santa Clara, CA 95052-8121.** Intel Corporation is an equal opportunity employer and fully supports affirmative action practices. Intel also supports a drug-free workplace and requires that all offers of employment be contingent on satisfactory pre-employment drug test results.*UNIX is a trademark of AT&T.

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The University of Sydney
AUSTRALIA

ELECTRICITY COMMISSION CHAIR OF POWER ENGINEERING

Reference No. 38/03

The successful candidate should have appropriate teaching, research and industrial experience in the field of electric power engineering. Preference may be given to applicants with a specific interest in sensors and instrumentation related to electric power.

The Chair receives generous support from the New South Wales Electricity Commission.

The School has teaching and research interests across the broad range of electrical engineering, including electronics, communications and computer engineering. It has a strong reputation in industrially-related research and wishes to expand its links into industry as well as to be a focus for high quality research.

The applicant may be asked to take on the role of Head of the School of Electrical Engineering from time-to-time and must therefore be able to demonstrate skills and a willingness appropriate to the role.

The University reserves the right to appoint by invitation and not to proceed with any appointment for financial or other reasons.

Further general information is also available from the Association of Commonwealth Universities, 36 Gordon Square, London, WC1HOPF.

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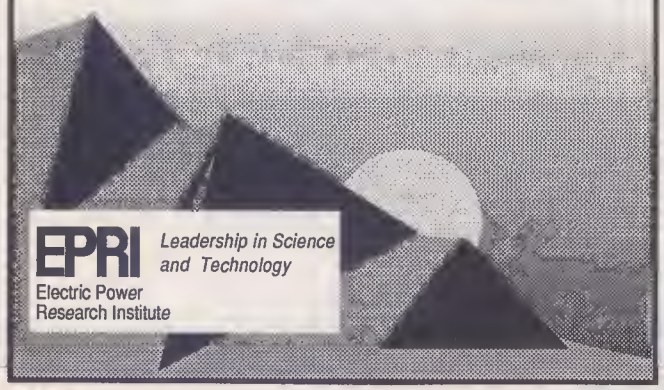
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The Center for Research in Electro-Optics and Lasers (CREOL) at the Univesity of Central Florida is seeking highly qualified applicants for a number of Graduate Assistantships in optics. Stipends range from $11,000 to $14,000 for 12 months. Exceptional students will be considered for assistantship enhancements up to $4,000 through the Litton Foundation and United Technologies Optical Systems. Degrees of MS and Ph.D. in Engineering and Physics are offered at UCF. CREOL has 28 faculty positions devoted to lasers and optical sciences and engineering. The academic program includes basic Electrical Engineering and Physics courses as well as, 23 specialized courses in electro-optics and lasers. Current research activities include: laser propagation, laser/material interaction, nonlinear optics, integrated-optics, infrared systems, optical signal processing, laser development, detector technology, ultrafast phenomena, x-ray sources and lithography, nonlinear optical spectroscopy, diffractive optics, thin film optics, metal vapor lasers, free electron lasers, optoelectronics, growth of nonlinear and laser host materials, superconductivity, solid state and micro lasers, and others.

Applications are invited from students with an excellent academic record and fluent command of the English language. Completed applications are due by March 15, 1991. To receive an application package, write to:

CREOL – University of Central Florida
Graduate Affairs Committee
12424 Research Parkway, Suite 400
Orlando, Florida 32826

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- Network security
- Accreditation of trusted systems
- DoD 50200.28 criteria

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- Development of trusted systems, software, databases, operating systems or communications
- 2+ years in a computer security role, ideally in an IBM mainframe environment

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- 3+ years experience with satellite or ground systems

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- 3+ years experience with digital transmission of data-voice-video, voice-data encryption, digital coding

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ARGONNE NATIONAL LABORATORY

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A Master's or Ph.D. in E.E. or Physics and 1-5 years experience with low-level microwave design techniques or particle beam applications are necessary. **(Box# 37995)**

RF ENGINEER

A Ph.D. in E.E., 5 years experience and considerable knowledge of electromagnetic theory and high frequency RF design and analysis techniques are required. **(Box# 82984)**

ELECTRICAL ENGINEER

A B.S.E.E. and 5-10 years experience with RF circuitry and techniques are necessary. **(Box# 36626)**

ASSISTANT ELECTRICAL ENGINEER

An advanced degree in E.E. and at least 4 years work experience are imperative. Knowledge and experience with the design and operation of pulsed and steady-state high current power supply systems is important. **(Box# 82717)**

MECHANICAL ENGINEER

A B.S. or M.S. in M.E. and approximately 10 years experience in vacuum technology and the fabrication and machining of materials. **(Box# 36620)**

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M.S./Ph.D. or equivalent plus 5-10 years experience and considerable knowledge and experience in opto-mechanical design are required. **(Box# 82976)**

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Requires a Ph.D. in Physics and 1-5 years experience with various accelerator systems. **(Box# 81203)**

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Each of these positions commands an excellent salary and benefits package. Confidential consideration can be obtained by sending your resume, indicating position of interest, to: **Walter D. McFall, Box J-APS-(Box#)-33, Employment and Placement, ARGONNE NATIONAL LABORATORY, 9700 South Cass Avenue, Argonne, IL 60439.** Argonne is an equal opportunity/affirmative action employer.

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The electronics program has traditionally been an important one in the College of Engineering at Washington State University, receiving the support and respect of many leading industries. Recently a group of five such industries—Tektronix, Eldec, John Fluke Co., Data I/O, and Hewlett-Packard have cooperated with the state of Washington to create an endowment for a Distinguished Professorship in Analog Electronics. We are seeking applications and nominations for the position.

The distinguished professor will be an active participant in the established NSF Industry/University Cooperative Research Center for Design of Analog-Digital Integrated Circuits. This center is sponsored by the NSF and also has significant industrial support. This position will actively interface with the center's personnel and its research programs.

The person fill this position must have:

- An appropriate doctoral degree or equivalent qualifications.
- Evidence of research in analog electronics and the capability to assume a role of leadship
- Ability to effectively teach undergraduate and graduate courses.
- Proven ability to work cooperatively with academia, the electronics industry, and government agencies.

Washington State University is a land-grant university located in the beautiful rural area of eastern Washington state offering outstanding quality of life. The ECE Department offers programs leading to the B.S., M.S., and Ph.D. degrees with areas of strength which includes analog and digital electronics, VLSI and computer engineering. Approximately 100 B.S. degrees per year are awarded and the department has an enrollment of approximately 80 full-time graduate students.

Letters of nomination and/or applications should be sent to:

Dr. Yacov Shamash, Chairman
Electrical and Computer
Engineering Department
Washington State University
Pullman, WA 99164-2752

Applications should include a complete professional vita and list of references. Additional information is available to interersted applicants. Screening of applicants will begin December 15, 1990. Position effective August 16, 1991. Washington State University is an equal opportunity, affirmative action employer and educator. Protected group members are welcome to apply.

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Advanced Analog Design. Develop mixed analog/digital microelectronics for high resolution data acquisition/signal conditioning, and new sensor technology.

Digital Communication Networks and Systems. Design and analyze real time digital networks and digital Land Mobile Radio systems. Networks research emphasizes protocols and structures; LMR research emphasizes modulation and coding as well as detection and new system concepts.

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DEAN

School of Engineering and Applied Science

Applications and nominations are invited for the position of Dean, School of Engineering and Applied Science.

The Dean is the chief executive officer of the School and is expected to provide vision and leadership in advancing the interests of the school. The new Dean will be a person who can forge strong cooperative working relationships with faculty and university administrators, and will facilitate the generation of, and support of, programs with key government and business entities.

Candidate should possess the following qualifications:

- An earned doctorate in engineering or science-related field
- A distinguished record as a scholar showing commitment to teaching and research
- Demonstrated administrative ability
- Effective interpersonal and communications skills
- Demonstrated ability in obtaining sponsored research support from government and industry
- Ability and interest in fund-raising activities
- Activity in scholarly and professional organizations
- Commitment to continuing and cooperative education

The School of Engineering and Applied Science is one of eight schools within The George Washington University, located in the Foggy Bottom section of Washington, D.C., close to the White House, Kennedy Center and other prominent national monuments. It consists of the Departments of Civil, Mechanical, and Environmental Engineering; Electrical Engineering and Computer Science; Engineering Management; and Operations Research. Within the purview of these departments, several off-campus graduate teaching and research programs are offered. The School will be a major component of the university's new Northern Virginia research/education center.

Application materials should include a cover letter summarizing outstanding qualifications for the position and a current resume. Review of applications and nominations will commence immediately and continue until the position is filled. The intended starting date for the position is July 1, 1991. Salary and benefits are competitive. Send materials to:

Engineering Dean Search Committee
Attention: Ms. Cleo Graves
Room 801, Rice Hall
The George Washington University
Washington, DC 20052

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JPL/NASA VISITING SENIOR SCIENTIST PROGRAM

EARTH SCIENCE AND APPLICATIONS DIVISION

Information Management

The Jet Propulsion Laboratory is seeking a senior scientist to provide staff expertise in information systems with emphasis on techniques, approaches, and standards relating to distributed information management, to provide advice to the Earth Science and Applications Division on matters regarding technological and funding aspects of NASA's interdisciplinary approach to information and data management. Experience gained, techniques developed, standards tested and adopted in the course of this effort will be incorporated into versions of EOSDIS to be provided by the EOSDIS Core System contractor. Duties include development and execution of program level plans for EOSDIS information management, technical guidance, advice, and coordination of activities with relevant NASA centers, university, and international groups, and EOSDIS program managers and science program managers within NASA headquarters. Requires a Ph.D. or equivalent experience and training in computer science and information systems, and a minimum of two years experience beyond the Ph.D. in research and/or teaching information systems approaches and techniques. Good written, oral, and presentation communication skills are essential, as is the ability to manage research and development tasks.

Tenured faculty members are the preferred choice, although qualified individuals from non-profit research institutions may also be considered. This position is open for immediate filling. Normal assignment in the Visiting Senior Scientist Program does not exceed two years. Appointees must be U.S. citizens or permanent residents and are expected to return to their home institution following the NASA assignment.

Please provide a curriculum vitae, bibliography, and the names of four references to: Dr. Harry Ashkenas 183-900, Jet Propulsion Laboratory, 4800 Oak Grove Drive, Pasadena, California 91109, (818) 354-8251. Equal Opportunity Employer.

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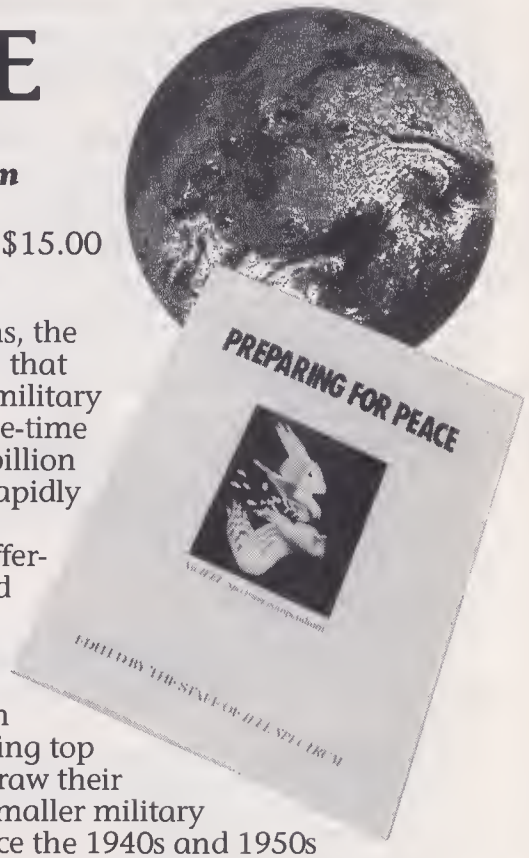
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With one in three EEs in the United States directly or indirectly affected by the military—and 10 percent or more of the total national manufacturing output devoted to military uses—the potential impact of this cutback on the industry is formidable.

This special report, "Preparing for Peace," excerpted from the November 1989 issue of SPECTRUM focuses on ways the industry is coping with this emphasis on peace and shows how some companies are attempting to reallocate their resources—and the skills of their scientists and engineers. Highlighted are the economic factors concerning science and research that must be faced, the technologies and areas likely to attract increased attention, and the military and international implications of the retrenchment.

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U.S. AIR FORCE LABORATORY GRADUATE FELLOWSHIP PROGRAM

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APPLICATION DEADLINE: January 16, 1991
APPOINTMENTS BY: March 31, 1991

INTRODUCTION: The Air Force Office of Scientific Research (AFOSR) has established a fellowship program for graduate studies at U.S. institutions offering the Ph. D. in appropriate fields. Twenty-five fellowships will be awarded each year.

ELIGIBILITY: Applicants must be U.S. citizens with bachelor's degree by September 1991. Applicants will be evaluated without regard to age, sex, race, religion, or national origin.

TERMS: Stipends of $15,000, $16,000, and $17,000 will be paid for the first, second, and third years of the program respectively. AFOSR will provide full tuition and required fees and $2,000 to the Fellow's department. Fellows will be responsible to and paid by the academic institution. The sponsor favors the use of these funds to support the student's research.

TENURE: The normal Laboratory Fellowship schedule is for 36 months during 3 consecutive years. Under exceptional circumstances, the fellowship may be scheduled for 36 months within 5 consecutive years, upon approval by sponsor.

Laboratory Graduate Fellowships awarded under this program will be for study in the following disciplines:

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Electrical Engineering
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Industrial and Civil Engineering
Life Sciences, Biology and Biophysics
Materials Science, Ceramic Engineering, and Metallurgy
Mathematics
Mechanical Engineering
Physics

For information and applications contact:
SCEEE - Fellowship Program
1101 Massachusetts Avenue
St. Cloud, FL 34769
Phone: (407) 892-6146
FAX: (407) 957-4535

Information and application materials provided will cover all Department of Defense Graduate Fellowship Programs.

Circle No. 31

The University of Sydney

AUSTRALIA

SENIOR LECTURER

Electrical Engineering Foundation

Reference 37/02

The Electrical Engineering Foundation has established a project on "Continuing Engineering Education for Electrical Technology." This is supported by the major electrcial industries and sponsored substantially by the NSW State Education and Training Foundation. The aim is to develop a continuing education program for professional engineers covering the key areas in electrcial engineering.

The appointment is for one year in the first instant with the possibility of appointment for up to three years if funds are available. The appointee will have the day to day responsibility for the planning and presentation of courses and continuing education activities like short courses and seminars in support of the overall program under the general guidance of the program manager.

A degree of higher degree in Electrical Engineering is required preferably with some teaching and practical experience. Skills in presentation and organization are essential. Further information can be obtained from Professor HK Messerle 612 692 2565.

Salary: $A43,984–$A51,015 per annum according to qualifications and it may also be supplemented by a market loading.

Closing: 8 November 1990.

Method of application: Applications quoting Reference No., and including curriculum vitae, list of publications and the names, addresses and fax nos., of three referees (only three referees will be contacted in the first instance and if more referees are nominatd they should be ranked in order of preference) to the Registrar, Staff Office, University of Sydney, NSW 2006 Australia by the above date.

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BSEE, 2 years experience in line or project management, 5 years in instrumentation design, a broad physical science background, and analog/digital and microprocessor-based design experience required. NASA/military program and CAE experience preferred.

We offer a competitive compensation package. Send your resume and salary history to: **KMS Fusion, Inc., code 90-026-IEEE, 700 KMS Place, P.O. Box 1567, Ann Arbor, MI 48106.**

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As part of Motorola's Corporate R&D Laboratory based in the Chicago area, we are looking for an individual with a M.S. or Ph.D. in Computer Science and with a minimum of 5 years hands-on experience of applying Artificial Intelligence techniques in solving real-world problems.

The ideal candidate should also have working knowledge of emerging software technologies including Knowledge-Based Software Assistant (KBSA), Computer-Aided Software Engineering (CASE), Object-Oriented Design and Programming, Software Reverse Engineering and Reengineering.

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Our TEAS Group (Technical and Engineering Acquisition Support) provides the Air Force Munition Systems Division at Eglin Air Force Base with highly specialized support for its weapons acquisition process, from concept exploration through production and deployment.

We are seeking Electro-Optical Instrumentation Engineers to design, analyze and test high speed and resolution imaging devices/systems; document results in technical reports; and work directly with government and other contractors as part of an integrated program effort.

Requirements include a BS/MS or PhD (EE, Physics, Optical Sciences or Applied Optics) with a minimum of 3-4 years experience encompassing electronic imaging devices/systems, CCD's, electro-optics, imaging, optical sensors, focal plane arrays and photon detectors.

Qualified applicants are invited to send a complete resume in strict confidence to: **Sverdrup Technology, Inc., Human Resources Manager, TEAS Group, BT049, P.O. Box 1935, Avenue D and Fourth Street, Building 260, Eglin AFB, FL 32542-5000**

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Arkansas Nuclear One, Mike Brock, Route 3, Box 137-G, Russellville, AR 72801. (501) 964-5034, FAX (501) 964-5037.

Waterford/3, Newton Spitzfaden, P.O. Box B, Killona, LA 70066. 1-800-535-7494, FAX (504) 464-3262.

EEO/AA/M/F/H/V.

Entergy Operations

WASHINGTON STATE UNIVERSITY

The Department of Electrical and Computer Engineering at Washington State University invites nominations and applications for the **Boeing Endowed Chair in Computer Engineering**, effective August 16, 1991.

Washington State University seeks an individual who has made significant contributions to the field of **Computer Engineering** to fill the chair endowed by the Boeing Company. The preferred candidate would be one whose primary interests are in computer systems design (e.g., networking, neural networks, high integrity systems, real time systems, computer architecture, CAD). Nominations of candidates from both industry and academia are welcome. A significant record of research funding and publications is expected.

The Department actively participates in a number of research projects that are funded by the Washington Technology Center (WTC). The WTC was established by the State of Washington in 1983 to help promote research programs in the State's research universities that will be of benefit to the industrial sector in the State of Washington. The biennial budget for the Center currently exceeds $20 million. The individual chosen, will be expected to play a leading role in the WTC Computer Systems and Software Technology program which currently has a budget of over $2.7 million for the biennium.

Recently, the Department has established an NSF Industry/University Cooperative Research Center for Design of Analog-Digital Integrated Circuits. This Center is currently sponsored by the NSF, WTC and 14 industrial companies. Depending on the area of specialty it is hoped that the Boeing Chair in Computer Engineering will actively interface with the Center personnel and its research programs.

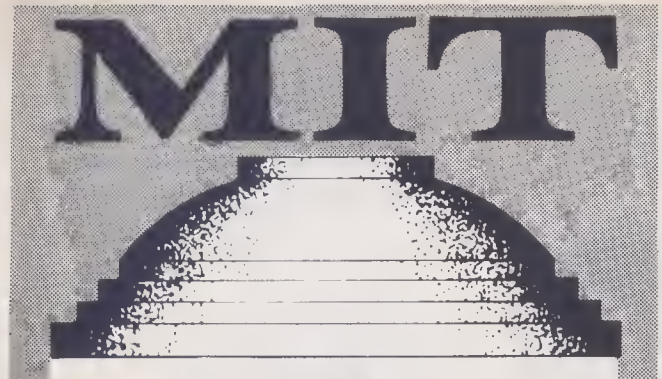
Candidates for this position must be capable of providing leadership for the continued expansion of the Computer Engineering program within the Department. As a tenured and distinguished Professor, the individual filling the position will be expected to teach, conduct funded research, and direct Ph.D. and M.S. student research programs. An earned doctorate in engineering or a related discipline is required.

The Department of Electrical and Computer Engineering has full breadth undergraduate and graduate programs, offering the B.S., M.S. and Ph.D. degrees. Major research and academic programs exist in computer engineering, computer science, systems and controls, electronics and solid state, power, and electromagnetics. The Department recently moved into a new building with expanded research and academic facilities. There are 310 certified (junior and senior) undergraduate majors and 130 graduate (M.S. and Ph.D.) students in residence on the Pullman campus. Additionally, the department has resident undergraduate and graduate programs with 110 students in Richland, Washington. Collaborative research exists between the computer engineering faculty and mechanical engineering faculty in the area of manufacturing and robotics. Research and collaborative ties exist also with faculty at the University of Washington, the University of Idaho, and Oregon State University. Close working relationships exist between the university and the electronics industry of the Northwest.

Letter of application, vita, and the names and addresses of at least three references should be addressed to:

Dr. Yacov Shamash, Chairman
Electrical and Computer
Engineering Department
Washington State University
Pullman, WA 99164-2752
Tel: (509) 335-8148 Fax: (509) 335-3818

Washington State University is an Equal Opportunity/Affirmative Action educator and employer. Protected group members are encouraged to apply.



Assistant/Associate Professors (2)

Underwater Vehicle Technology: Candidates should have a working knowledge, based on experience and/or advanced education (typically including a doctorate), that prepares them for teaching and research in one or more of the following areas: (1) vehicle propulsion and control; (2) tether dynamics; (3) new hull-design concepts for extreme ambient pressure; (4) materials and fabrication techniques for deep-ocean vehicles; (5) layered-control and other relevant AI systems; (6) underwater sensors and communications. While any of these areas could be appropriate specialties in support of the Department's programs, candidates should also be knowledgeable about system-design issues relating to unmanned underwater vehicles. The Department collaborates with the MIT Sea Grant Program and with other organizations in the development of working vehicles as well as on fundamental concepts and subsystems. Teaching responsibilities will include undergraduate and graduate education in deep-sea technologies and supervision of student research in a broad range of ocean engineering, including underwater systems dynamics, ocean sensing and information systems, and ocean acoustics.

Ocean Acoustics: Candidates should have a working knowledge, based on experience and/or advanced education (typically including a doctorate), that prepares them for teaching and research in one or more of the following specialties: (1) propagation of sound in the ocean; (2) acoustic scattering processes in the ocean; (3) ambient noise mechanisms; (4) oceanography; (5) communication, information, and sensing systems; (6) marine geology or geophysics. The Department's programs in this area include theory, computer modeling, and experiments (both laboratory and at sea). Candidates may have experience and interests that focus on any of these approaches, but they must be willing and able to work in a group that encompasses all of them, since the Department participates in major ocean acoustics programs (often with the Woods Hole Oceanographic Institution and other organizations). Teaching responsibilities will include graduate education in acoustics and supervision of student research in a broad range of ocean engineering, including underwater systems dynamics, ocean sensing and information systems, and deep-sea engineering.

Interested candidates should submit a cover letter and resume to: **T. Francis Ogilvie, Massachusetts Institute of Technology, 77 Massachusetts Avenue, (S-228) Cambridge, MA 02139.**

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Massachusetts Institute of Technology

HEAD

DEPARTMENT OF ELECTRICAL ENGINEERING
TEXAS A&M UNIVERSITY

Texas A&M University invites nominations and applications for the position of Head of the Department of Electrical Engineering. The Department has experienced continuous and significant growth for more than a decade, and currently has 52 tenure track faculty and 8 lecturers, 300 graduate students and 700 undergraduate students (Sophomore through Senior). The department has a research budget of $3.5M with current emphasis on communication and control systems, circuit theory, computer engineering, electromagnetics, electro-optics, electronic materials, microelectronics, microwaves, power systems, signal processing, solid state electronics and VLSI.

The Department Head will be expected to provide leadership for the growth and development of the Department and for encouraging the development of teaching, research and public service. The Head is responsible directly to the Dean of the College of Engineering and holds the rank of Professor of Electrical Engineering with tenure. Candidates should hold an earned doctorate in engineering, have an established reputation as a scholar and educator, and possess strong proven leadership ability with demonstrated administrative skills. Letters of application should include a current resume and names and telephone numbers of five references. Applications will be accepted until the position is filled. Screening will begin in January 1991 with an anticipated starting date of September 1991. Nominations or applications should be sent to:

Dr. Walter Haisler
Chairman, Department Head Search Committee
Department of Aerospace Engineering
Texas A&M University
College Station, TX 77843-3141

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Call for Papers

MILCOM '91 is soliciting both unclassified and classified papers (up to the level of Secret that have received foreign disclosure approval) on military communications for presentation at the MILCOM '91 conference and for publication in the conference Proceedings. Papers concerned with the conference theme of "Military Communications in a Changing World", as applied to systems, subsystems, technology, or operations are especially sought, but all papers related to Military Communications are welcome at this conference. Subject matter may include theoretical analysis, simulation, design, or measurements. Note that all U.S.-authored classified papers presented at MILCOM '91 must be preapproved for public release by the DOD cognizant release authority.

Author's Schedule:

Notice of intent and abstract due	November 15, 1990
Draft paper due	March 15, 1991
Final author notification	May 1, 1991
Camera-ready copy due	July 1, 1991

Send all Abstracts, Intent Notices, and Unclassified submissions to:

Dr. Albert E. Babbitt
Technical Program Chair
TRW Federal Systems Group
12450 Fair Lakes Circle
Fairfax, VA 22033

Send U.S.-Authored Classified submissions to:

Dr. Robert E. Lawrence
Technical Program Co-Chair
The MITRE Corporation, MS Z509
7525 Colshire Drive
McLean, VA 22102-3481

Send Foreign Authored Classified submissions to:

Dennis E. Litchfield
Office of the Assistant Secretary of Defense (C^3I)
The Pentagon, Room 3D 228
Washington, D.C. 30301-3040

Please submit a one-page unclassified abstract and five copies of the draft manuscript per the above schedule. With the abstract, include author names, affiliations, addresses, and phone numbers, and indicate which author is to be the point of contact for conference correspondence and whether the paper is to be presented in the classified or unclassified program. For additional information, contact Dr. Albert E. Babbitt, (703) 968-2000, Dr. Robert E. Lawrence (703) 883-7348 or Dennis E. Litchfield (202) 697-4541.

Sponsored by Institute of Electrical and Electronics Engineers Inc., IEEE Communications Society, and Armed Forces Communications and Electronics Association. Security for the classified sessions is sponsored by the Department of Defense.

MILCOM 91

Computer art in Boston

Few realize how serious an undertaking computer art has become. Yet more than 2000 entries from 500 artists representing 20 countries were considered for the 1990 Siggraph Traveling Art Show by an international panel of artists and curators. Titled "Digital Image/Digital Photography," the collection went on view Oct. 23 at The Computer Museum in Boston.



"Papilloma Virus, Third Edition" Copyright 1989 (ART)^n Laboratory
The 1990 Siggraph Traveling Art Show

The 30 pieces selected reveal "aesthetic quality and a significant use of the computer" in the creation of the artwork or its presentation, or in the interaction between the piece and the viewer, explained art show chair Thomas E. Linehan, director of the Visualization Laboratory in the College of Architecture at Texas A&M University, College Station.

The two- and three-dimensional works include prints, paintings, plotter-drawings, glass sculpture, animations, and phscolograms (pronounced skol'o-grams), or three-dimensional photographs similar to holograms except for being in full color.

One of the phscolograms, shown above, is of a papilloma virus superimposed on a mammogram, with a cancer visible in the lower right. To create such an object, the artist starts with multiple views of a scene, each of which is cut into vertical columns. The columns are then interleaved and positioned behind a barrier strip, or line screen. Lines in the screen are spaced so that each eye sees a different view, which the brain fuses into one 3-D image. Moving the head left or right obviously changes the picture.

Scenes may be real or simulated—either real objects are captured on photographic film or videotape and then scanned into a computer, or artificial worlds are created using computer graphics. Computer processing yields a photograph-like image in digital form.

In the phscologram of the papilloma virus, the image has been printed as a full-color transparency on one side of a 50-by-60-by-7.5-centimeter piece of plexiglass; the barrier strip is mounted on the other side. The finished work is viewed in a light box.

The show at The Computer Museum in Boston runs through Feb. 1, 1991. It is actually a selection chosen from pieces displayed at the 10th Annual Siggraph Art Show, held in August during the 17th Annual Conference on Computer Graphics and Interactive Techniques in Dallas.

SUPERCONDUCTORS

See for yourself

High-temperature superconducting films of yttrium-barium-copper oxide (YBCO) are available on a variety of substrates from Colorado Superconductor Inc. The three-year-old company specializes in supplying materials that demonstrate superconductive phenomena at temperatures above that of liquid nitrogen.

A standard 5-by-10-millimeter YBCO film with a superconducting temperature (T_c) of 92 K) is US $200. Larger films up to 40 by 40 mm in area are also available. Thicknesses range from 10 to 100 micrometers.

According to the company, the films show excellent transition characteristics, Meissner effect, and infrared and magnetic field response. Stoichiometric, morphological, and electrical characteristics are available on request. So are still thicker films for thick-film circuit applications.

Other products include a US $175 superconducting battery kit built around a YBCO toroid that mimics the U. S. Navy's magnetic energy storage device, and solid shapes of YBCO and bismuth-lead-strontium-calcium-copper oxide (with a T_c around 100 K). All products are described in a brochure. *Contact: Colorado Superconductor Inc., Department P10, Box 8223, Fort Collins, Colo. 80526; 303-490-2787; fax, 303-490-1301; or circle 62.*

LASERS

Desktop laser optics

Four programs meant for optical resonator design and laser beam propagation calculations work on Macintosh desktops. From Stanford University in California, the package takes advantage of the Macintosh graphic interface along with optimized algorithms, such as the complex ray-matrix approach for paraxial systems, fast Fourier and fast Hankel transforms for optical beam propagation, and the virtual source approach for unstable resonators.

Calculations that previously required batch runs on mainframe computers can be carried out at the desk. In most cases, the programs follow theoretical approaches outlined in the text *Lasers* (University Science Books, 1986) by Professor A. E. Siegman of Stanford.

The ABCD program, for example, allows an optical system to be built as a succession of optical elements (lenses, mirrors, Brewster plates, and so on). The system can be edited on the Macintosh in the same way as text is edited by using the CUT, COPY, PASTE, CLEAR, and UNDO commands. Focal length, thickness, and other parameters for each element may be edited at any time or made variable. Each element may also be made misaligned or astigmatic.

Of the other programs, Fresnel propagates an arbitrary wavefront successively through such elements as a hard-edged aperture, an arbitrary mask, and an arbitrary paraxial system. VSource uses a virtual source to calculate higher- and lowest-order eigenmodes of hard-edged unstable resonators, and VRM implements analytical formulas for designing gaussian variable-reflectivity-mirror resonators.

The Paraxia package, as it's called, comes on an 800K-byte Macintosh floppy disk. A single-user academic version is US $150, an industrial version is US $500, and an industrial site license is US $2500. *Contact: Software Distribution Center, Stanford University, Stanford, Calif. 94305-6225; or circle 60.*

INSTRUMENTATION

Smartness in harness

An intelligent power IC from Texas Instruments Inc. reduces both the component count and the complexity of wiring harnesses in instrumentation systems. The 8-bit serial-in, parallel-out TPIC2801 driver has eight 1-ampere, 30-volt outputs that it can monitor simultaneously. It can identify faults, disable affected channels, and report the status of each output to a microprocessor via a single output. Other multi-output switches have but a single reporting flag, which does not locate the failure, according to the company.

The IC accepts inputs directly from a microprocessor or low-level logic, and can directly switch lamps, relays, printheads, small solenoids, and other medium-current or high-voltage loads. Also integrated on the chip is the self-protection circuitry required for active energy snubbing associated with inductive loads.

Fabricated in TI's BIDFET technology, which incorporates bipolar double-diffused and MOS field-effect transistors, the TPIC2801 operates from −40 °C to +105 °C and comes in a 15-pin single-inline package. Suggested resale price is US $3.20 each in quantities of 1000. *Contact: Texas Instruments Inc., Semiconductor Group, Box 809066, Dallas, Texas 75380-9066; 1-800-336-5236, ext. 700 (North America) and 1-214-995-6611, ext. 700 (elsewhere); or circle 61.*

BOOKS

Guides to business East and West

The American Electronics Association (AEA) has two books for those in the electronics industry on both sides of the Pacific. The 450-page 1990/91 AEA membership directory profiles some 2800 member firms and 500 associate members. Includ-

(Continued on p. 132)

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Circle No. 20

Faculty Search

Materials Science Materials Engineering

The MIT Department of Materials Science and Engineering has a search for a tenure track assistant professorship. A faculty member is sought with demonstrated potential, creativity and teaching ability in an aspect of the field of materials science and engineering. This position is open for a faculty member specializing in any of the materials classes (metals, ceramics, polymers or electronic materials), or more broadly in materials science or materials engineering.

Doctorate required and experience desirable. Salaries and benefits competitive. Position will be filled only if exceptional candidates are found. Appointment to a more senior position is possible based on experience and accomplishments. Send resume (include citizenship and/or visa status), publications list and references to **Professor Merton C. Flemings, Head, Department of Materials Science and Engineering, Massachusetts Institute of Technology, 77 Massachusetts Avenue, Cambridge, MA 02139.** MIT is an equal opportunity/affirmative action employer.

MIT

EES' TOOLS & TOYS

(Continued from p. 131)

ed are the names of top executives, number of employees, subsidiaries, products, and fax, telephone, and telex numbers.

For AEA members, beyond their membership allocation, the directories start at US $75 and move down to US $55 each for five or more. For nonmembers, the price is US $175 for one and down to US $155 each for five or more.

Soft Landing in Japan is an AEA primer for U.S. software firms and others seeking to maximize their business opportunities in Japan. The market-entry handbook was developed by the relatively new Software Subcommittee of the AEA Industry Committee in Japan.

Included is a market overview covering distribution, legal issues, recruitment, marketing, and customer support. There are also six case studies of U.S. software companies—Autodesk, Comshare, Ingres, Lotus, Oracle, and SDRC—that are successfully selling in Japan. The handbook is US $50 for AEA members, US $95 for nonmembers. *Contact: American Electronics Association, 5201 Great America Parkway, Santa Clara, Calif. 95054; 408-987-4200. Or, for the AEA directory, circle 63, and for the software handbook, circle 64.*

RAILROAD BUFFS

Model a railroad on computer

All aboard for a computer simulation program that mimics a train's operation and allows for to-scale modeling. Design Your Own Railroad allows model railroaders to design and test model layouts on an Apple II computer using Z, N, HO, S, G, and O scales. Layouts can be made complete with scenery, to-scale tracks (with selectable radii for curves), switches and railroad yards.

With the track creation completed, the user can put on an engineer's cap, step behind the controls of a locomotive pulling up to 16 cars loaded with valuable freight or paying passengers, and head for real destinations. The railroad has 46 cars.

Switcher locomotives can be used in the freight yards to couple and uncouple boxcars of manufactured goods, hoppers of coal or grain, tank cars of oil or chemicals, and flatcars.

The engineer relies on a mouse or joystick to select icons to control the speed, direction, and coupling/uncoupling of the train and 26 switches in the layout.

Suggested retail price of the Apple II version of Design Your Own Railroad is US $49.95. The program runs on 64K bytes and is available on 5.25- and 3.5-inch disks. Versions for the Macintosh and IBM Personal Computers will be coming down the tracks soon. *Contact: Abracadata, Box 2440, Eugene, Ore. 97402; 503-342-3030; or circle 65.*

JAPANESE TECHNOLOGY

Reports for the accessing

Need to know about Japanese technology? Then consider a trio of directories, each of which serves as a guide to Japanese technical information. The volumes are produced jointly by the U.S. Commerce Department's Japan Technology Literature Program and its National Technical Information Service (NTIS).

The *Directory of Japanese Technical Resources in the United States—1990* lists over 250 commercial services, government agencies and libraries that acquire, translate or disseminate Japanese technical information. Japanese reports translated at Federal expense in 1989 and 1990 and available to the public are also cited. Included as well are background articles discussing how to access the Japanese resources. The price of NTIS Order No. PB90-155730 is US $39.

The *Directory of Japanese Databases* describes 43 Japanese databases that are accessible from the United States. Included are the types of databases, contents, producer's name, address and telephone number, how to access, and the equipment required (NTIS Order No. PB90-163080; US $35).

The *Directory of Japanese Technical Reports* contains bibliographic citations (including abstracts) of Japanese reports added to the NTIS collection between January 1989 and March 1990. The directory is in the same format as the NTIS Government Reports Announcements and Index (NTIS Order No. PB90-163098; US $35).

The complete set (NTIS Order No. PB90-163072) is available for US $89. *Contact: U.S. Department of Commerce, National Technical Information Service, Springfield, Va. 22161; 703-487-4650; fax, 703-321-8547.*

More on Japanese technology

The Japan Technology Literature Program (JTLP) within the U.S. Department of Commerce has other sources of information about what the Japanese are up to. Its publication, the *Japanese Technical Literature Bulletin*, includes reports on technical and business studies, speeches, and product developments, and summarizes articles appearing in Japanese company newsletters.

JTLP, to give its full pedigree, is part of the Japan Technology Program in the office of International Policy and Programs under the Assistant Secretary for Technology Policy of the Technology Administration of the Commerce Department.

The technology program's mandate is to provide U.S. business and industry with information on scientific and technical developments in Japan. One of the first objectives of the program's director, Dr. Phyllis Genther, is to increase small and medium-sized U.S. companies' awareness of the program's goals and activities.

The literature program works closely with the National Technical Information Service (see previous item), from which most of the reports mentioned in the JTLP bulletin are available. A subscription to the bulletin, which comes out at least quarterly, is free. *Contact: Japan Technology Literature Program, Room 4817 HCHB, 14th and Constitution Avenue, Washington, D.C. 20230; 202-377-1288; fax, 202-377-4498.*

Coordinator: Alfred Rosenblatt

CLASSIFIED EMPLOYMENT OPPORTUNITIES

The following listings of interest to IEEE members have been placed by educational, government, and industrial organizations as well as by individuals seeking positions. To respond, apply in writing to the address given or to the box number listed in care of *Spectrum* Magazine, Classified Employment Opportunities Department, 345 E. 47th St., New York, N.Y. 10017.

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IEEE encourages employers to offer salaries that are competitive, but occasionally a salary may be offered that is significantly below currently acceptable levels. In such cases the reader may wish to inquire of the employer whether extenuating circumstances apply.

Academic
Positions Open

Caltech Electrical Engineering—The Division of Engineering and Applied Science of the California Institute of Technology invites applications for a tenure-track position in electrical systems. Candidates with broad interests in signal processing, as applied to speech and image processing, control, communications, sonar, radar, astronomy, etc., or to VLSI implementations of signal processing algorithms, are encouraged to apply. The successful candidate will be expected to develop an active research program and to teach undergraduate and graduate courses. Preference will be given to applicants at the Assistant Professor level, but exceptional candidates at higher levels may also be considered. Interested persons should send complete resume, including a description of research interests and the names and mailing addresses of at least three references to: Professor Robert McEliece, MS 116-81, California Institute of Technology, Pasadena, CA 91125. Caltech is an Affirmative Action, Equal Opportunity Employer. Women and minorities are encourage to apply.

Electrical Engineering: Bucknell University invites applications for a tenure-track position at the Assistant Professor level. The individual selected will also be the recipient of the T. Jefferson Miers Fellowship which will provide support for summer research and professional development. We are seeking an individual with promise as a teacher and researcher in the area of computer hardware and microprocesssors. Qualifications include a Ph.D. (by the time of appointment) in Electrical and/or Electrical/Computer Engineering. Bucknell University is a private university emphasizing quality undergraduate education in engineering and liberal arts. Review of applications will begin on November 1, 1990 and will continue until the position is filled. Send application to Maurice F. Aburdene, Electrical Engineering Department, Bucknell University, Lewisburg, PA 17837. Women and members of minority groups are especially encouraged to apply.

University of California, Santa Barbara, Electrical and Computer Engineering. Applications are invited for at least three tenure-track assistant professor positions, available effective 7/1/91, for candidates experienced in image processing/computer vision/speech processing, parallel algorithms, electromagnetics, or imaging technology (including optical processing). Normally, completion of a doctorate is required at the time of the appointment. Candidates should have an established research reputation or outstanding research potential, the ability to attract external research funding, and a strong commitment to teaching at the undergraduate and graduate levels. Applicants should send their resumes and the names and addresses of at least four professional references to: Faculty Search Committee, Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106. Applications will be received until the positions are filled. Proof of U.S. Citizenship or eligibility for U.S. employment will required prior to employment (Immigration Reform and Control Act of 1986). An Equal Opportunity/Affirmative Action employer.

University of Rochester, Electrical Engineering. The faculty is seeking applications from individuals who are active in digital signal processing, optocommunication systems, computer engineering, ASIC design, or related areas. These individuals would contribute to existing faculty groups in image & signal processing, ultrasound & medical ultrasound, superconducting electronics, ultrafast phenomena, computer systems, design automation, integrated circuit design & testing, and networking. Applicants should have an established research record, or a commitment to establish such a record. Those appointed are expected to develop independent or cooperative research efforts and participate in undergraduate and graduate teaching. Appointments are usually made at the Assistant Professor level, tenure track. However, higher level appointments may be made in exceptional cases. A Doctorate in Electrical Engineering or a closely related field is required. Applicants should send a full resume, a statement of research plans, and copies of relevant publications to: Professor Edwin Kinnen, Chair, Dept. of Electrical Engineering, University of Rochester, 517 Computer Studies Bldg., Rochester, NY 14627. The University of Rochester is an Equal Opportunity Employer (M/F) and specifically invites and encourages women and minorities to apply.

Faculty Positions. Cleveland State University is seeking applications for a tenure track faculty position in Electrical Engineering. Appointment will be at the Assistant or Associate Professor level with a competitive salary and rank commensurate with qualifications. Qualifications include a Ph.D. degree, the abilities to teach in B.S., M.S., and Doctoral-level programs and to engage in a vigorous research program. Specialities desired are in communications, signal processing and computer engineering. Primary departmental interests are in information theory, coding, signal processing, image processing and all areas of computer engineering. Faculty members in the department have the possibility of obtaining research support for industry-sponsored projects locally through the CSU Advanced Manufacturing Center. NASA Lewis Research Center is an additional local source of research support. Deadline: November 25, 1990 or when position is filled, with ongoing screening of applications. Starting date: September 16, 1991. Send resume and list of three references to: Dr. James H. Burghart, Chairman, Electrical Engineering Department, Cleveland State University, E. 24th & Euclid Ave., Cleveland, OH 44115. Equal Opportunity Employer, m/f/h.

The Johns Hopkins University, Department of Electrical and Computer Engineering, invites applications for tenure-track faculty positions, at the Assistant or Associate Professor level, in the general area of signals and systems. Preference will be given to candidates with research interests in signal processing. Candidates for Associate Professor appointments are expected to have significant research records. Candidates for Assistant Professor appointments are expected to show strong research potential. Tenured appointments at the level of Professor are also possible for uniquely qualified individuals. Positions may be filled as early as January, 1991. Applicants should send resumes, including names of at least three references, to Professor H.L. Weinert, Department of Electrical and Computer Engineering. The Johns Hopkins University, Baltimore, MD 21218. The Johns Hopkins University is an equal opportunity/affirmative action employer.

Research Associate, Microwave CAD. The NSF I/UCR Center for Microwave/Millimeter-Wave CAD at the University of Colorado, Boulder has a post-doctoral opening for research in the area of computer-aided design of microstrip antennas. The position requires a Ph.D. in Electrical Engineering or a related field. The candidate must have a strong background in CAD techniques suitable for microstrip antennas and arrays with a dielectric layer covering, preferably having worked on a Ph.D. thesis in this field. Also, complimentary expertise in CAD of microstrip circuits is desired. The candidate should be capable of handling research contracts and should be able to supervise graduate students on research projects. Teaching responsibilities may also be assigned as needed. The initial appointment is for a minimum period of one year with the possibility of renewal. The salary will be in the range of $37.5K to$40K, depending upon relevant experience. To apply, send a resume (with names of references) to: Director, MIMICAD Center, University of Colorado at Boulder, Campus Box 425, Boulder, CO 80309-0425. Deadline for applications is October 15, 1990. The university of Colorado at Boulder has a strong institutional commitment to the principle of diversity in all areas. In that spirit, we are particularly interested in receiving applications from a broad spectrum of people including women, members of ethnic minorities and disabled individuals.

The Department of Electrical Engineering at the University of Maine invites applications at all ranks for a tenure track position in power engineering beginning January or September, 1991. Applicants should have an earned doctorate. The successful candidate will be expected to contribute to undergraduate and graduate teaching in the electric power area and to establish a research program. Opportunities exist to cooperate with several local power companies. Salaries are competitive and arrangements are made to assist junior faculty in initiating a research program. Applicants must send a resume which clearly indicates citizenship/visa status, a statement concerning teaching and research interests and a list of three references to: EE Search Committee, Barrows Hall, University of Maine, Orono, ME 04469. Applications from women and minorities are particularly encouraged. Review of applications will begin immediately and continue until February 15, 1991 or until the position is filled. The University of Maine is an Equal Opportunity/Affirmative Action Employer.

University of Toronto Department of Electrical Engineering. The Department of Electrical Engineering invites applications for two tenure-stream Assistant Professor positions in the area of Computer Engineering, available Immediately. Subareas of specialization include, but are not limited to, software engineering and computer architecture. Cross-appointment to the Department of Computer Science is a possibility. These positions involve both research and teaching at the undergraduate and graduate levels. Applicants must have a doctoral degree in Electrical Engineering, an outstanding academic record and effective teaching ability. These positions are two of several made possible by the expansion of the new Department of

Electrical Engineering and the establishment of a new undergraduate program in Computer Engineering. Applicants should send a curriculum vitae, a statement concerning teaching and research interests, and a list of three references to: Professor A.S. Sedra, Chairman, Department of Electrical Engineering, University Toronto, Toronto, Ontario, Canada M5S 1A4. In accordance with Canadian Immigration requirements, priority will be given to Canadian citizens and permanent residents of Canada. The University encourages both women and men to apply.

University of Minnesota, Minneapolis, Minnesota. The Department of Electrical Engineering invites applications and nominations for tenure track and tenured positions of all ranks. In addition for the 1991-92 academic year several visiting and temporary positions are available. The duties of tenure and tenure track faculty include the establishment of a sponsored research program and teaching at both the undergraduate and graduate level. Candidates with exceptional qualifications in all areas of electrical engineering will receive due consideration. Of particular interest, however, are individuals whose specialties lie in the areas of computer architecture and digital electronics, circuits, and VLSI design, and microelectronics, with particular interests in optoelectronics, or micromachining. The Department of Electrical Engineering has 46 faculty members providing undergraduate and graduate education and pursuing research in all areas of electrical engineering. The State-funded Microelectronics and Information Sciences Center and the Supercomputer Institute at the University of Minnesota provide opportunities for interdisciplinary research. The Department has a complete integrated circuit fabrication and design laboratory. Faculty have direct access to the full range of computing facilities including supercomputers. The requirements for all positions include an earned Doctorate in an appropriate discipline at the time of the appointment and outstanding academic and research records. Rank and salary will be commensurate with the qualifications and experience of the selected candidates. Applications and nominations should be sent with a resume containing the names of three references to: Professor Larry L. Kinney, Chairman of the Faculty Recruiting Committee, Department of Electrical Engineering, University of Minnesota, 200 Union Street SE, Minneapolis, MN 55455. The last date for receiving applications will be August 30, 1991 for positions available September 16, 1991. Review and interviews may begin as early as November 15, 1990, and early decisions can be made on positions. The University of Minnesota is an equal opportunity educator and employer and specifically invites and encourages applications from women and minorities.

Princeton University Dean, School of Engineering and Applied Science. Princeton University is seeking a Dean for the School of Engineering and Applied Science for an appointment to begin the Fall of 1991. Applications or nominations should be received by November 1, 1990, and should be sent to: Dean of the Faculty, 9 Nassau Hall, Princeton University, Princeton, NJ 08544. Princeton University is an affirmative action, equal opportunity employer.

Wayne State University anticipates openings for visiting, tenure-track or tenured faculty in the Electrical and Computer Engineering Department. We are seeking research oriented individuals interested in either: computer engineering, with emphasis on networks, parallel and distributed processing, modeling and performance analysis; VLSI design; optics; communications; or control. Applicants should have an earned Ph.D. and be committed to teaching and research. Rank and salary will depend on experience and qualifications. Wayne State is a large urban university, and welcomes applications from women and minorities. Resumes should be sent to Dr. M.P. Polis, Chair, ECE Dept., Wayne State University, Detroit, MI 48202. Wayne State University is an Equal Opportunity/Affirmative Action employer.

Bellmon Chair in Photonics Oklahoma State University School of Electrical and Computer Engineering. Oklahoma State University invites nominations and applications for the Henry and Shirley Bellmon Chair in Photonics. The successful candidate will have an established reputation as a scholar, a demonstrated capacity for leadership and a sincere interest and ability to develop multi-disciplinary faculty and student programs in Photonics. The person who is selected for this position will hold a tenured position in the School of Electrical and Computer Engineering and will teach courses relating to their interests at the graduate and undergraduate levels. The person will work very closely with the faculty in the Department of Physics and will participate in the research program of the OSU Center for Laser Research. Applicants should have received an earned doctorate with at least one degree in Electrical Engineering and should have a strong background in academic and/or industrial research in the application of optical technology to problems in areas such as communications, computation or surveillance. The OSU Center for Laser Research was established in 1988 to focus optical research in a nationally prominent program with faculty from Physics, Chemistry and Electrical Engineering. A new building has recently been completed with 9,100 square feet of prime research space already occupied by the Center. Current projects being conducted by the Center are funded from the federal government, the State of Oklahoma and private industry. Oklahoma State University has made a substantial commitment to the Center and to the Henry and Shirley Bellmon Chair which is funded by an endowment of one million dollars. Nominations and applications, including a curriculum vitae should be sent to: Professor James Baker, School of Electrical and Computer Engineering, 202 Engineering South, Oklahoma State University, Stillwater, OK 74078-0545.

Electrical and Computer Engineering. The Department of Electrical and Computer Engineering at West Virginia University anticipates possible faculty positions in all areas. Salary and rank will be commensurate with qualifications. Positions will be tenure track. Applicants must have the Ph.D., must have potential for high quality teaching, and will be expected to initiate research and participate in departmental research programs. A curriculum vitae and cover letter identifying an area of specialization should be sent to: Virginia University, P.O. Box 6101, Morgantown, WV 26506-6101. Applications will be received and considered immediately and searches will continue until all available positions are filled. West Virginia University is an affirmative action/equal opportunity employer m/f.

Computer Engineering Department, San Jose State University, invites applications for tenure track faculty positions 91-05, 91-06. Earned doctorate in Electrical or Computer Engineering is required. Areas of interest for 91-05 are (A) computer hardware and digital design (B) operating systems and compiler design. Hardware design experience is required for 91-06 areas of interest: (1) hardware and software design of CISC, RISC, and stack machines (2) memory hardware and software design including cache and EDC (3) graphics hardware and software design. Rank and salary consistent with qualifications and experience. Open period is from 9-1-90 until positions are filled. Please send a letter of intent, a complete curriculum vitae, and names & telephone numbers of three references to Dr. Nicholas L. Pappas. Chair, Computer Engineering Department, San Jose State University, San Jose, CA 95192-0085. SJSU is an equal opportunity, affirmative action, Title IX employer.

Electronic Engineering Technology: New Mexico Highlands University is seeking an Assistant or Associate Professor in Engineering Technology for January 1991 or August 1991. The candidate will teach beginning and advanced courses in a BS degree program in electronic and computer engineering technology. Duties will include development of new courses and laboratories. Areas of preference include microprocessor systems/interfacing, electronic devices, digital communication systems, and the UNIX Operating System. A Ph.D. in Electrical or Computer Engineering preferred, however, a candidate with an MS in Electrical or Computer Engineering will be considered. Salary range is $28,000 to $36,000. Applications will be accepted until the position is filled. Forward a resume, letter of intent along with the addresses of three references to: Dr. Calvin Thomas, Chairperson, Search & Screen Committee, School of Science & Technology, New Mexico Highlands University, Las Vegas, NM 87701 (505) 454-3458 AA/EEO Employer.

Department of Electrical and Computer Engineering. Ecole Polytechnique de Montreal invites nominations and applications for candidacy of The Videotron industrial chair in Broadband Telecommunications Technology. Of particular interest are candidates with a strong research background in broadband communication systems with a special emphasis on cable and fiber optics distribution networks and/or video technologies. Candidates for the position must be capable of providing leadership in collaborative research with industry and contributing significantly to the research activities and graduate student supervision in the Department of Electrical and Computer Engineering at Ecole Polytechnique. The chair will allow its holder to assemble and lead a team of researchers and graduate students involved in broadband high speed communication, integration of voice, data and video on cable and fiber optics distribution networks, video technologies and services, and modelling and performance analysis. Applicants and nominees must have an outstanding research record, a strong interest in teaching, and a commitment to the creation and development of a world-class research program in broadband telecommunications. The chair will be sponsored jointly by Videotron and a federal granting agency. To that effect, the candidate selected to become the chairholder will first prepare a detailed research proposal for approval by this granting agency. Upon approval, the candidate then becomes the chairholder and will join the Communications Section of the Department of Electrical and Computer Engineering of Ecole Polytechnique. The chairholder will hold a tenure track position at Ecole Polytechnique, normally at the level of full professor. He/she will participate in teaching activities and will have privileged access to the expertise and facilities of Videotron. A working knowledge of French would be an asset. Interested persons should write or call Professor David Haccoun, Chairman of the Search Committee for the Videotron Industrial Chair In Telecommunications, Ecole Polytechnique, Department of Electrical and Computer Engineering, P.O. Box 6079, Station A, Montreal (Quebec) Canada, H3C 3A7. Tel.: (514) 340-4548. Fax.: (514) 340-4562. Applications accepted until December 3, 1990 or until candidate is selected.

Director, Biomedical Engineering. The Johns Hopkins University School of Medicine and The Johns Hopkins Hospital are seeking a scientist to lead the Department of Biomedical Engineering. Applicants should have demonstrated leadership qualities and outstanding abilities in research and teaching in the application of engineering to problems of medical science. Please send letter of application, curriculum vitae, and bibliography to: William R. Brody, M.D., Ph.D., Chairman, Biomedical Engineering Search Committee, Johns Hopkins Hospital, Department of Radiology, B1-119 Tower Radiology, 600 North Wolfe Street, Baltimore, Maryland, 21205. An Affirmative Action/Equal Opportunity Employer.

Wright State University Department of Computer Science and Engineering, Dayton, OH 45435. Applications are invited for the position of Instructor in Computer Science and Engineering. Successful candidates must have an M.S. degree in Computer Science, Computer Engineering, or related field. Teaching experience strongly preferred as duties will include teaching introductory undergraduate courses in computer science/ engineering, preparing classroom materials, grading, and advising. Instructor positions are non-tenure track, nine-month appointments with the likelihood for reappointment. Summer support is usually available for qualified instructors. There are opportunities for pursuing a PhD. Wright State University's Computer Science and Engineering department has a variety of dynamic research and education programs. Its laboratory facilities boast a VAX 5810, 30 SUN and DEC workstations networked into extensive University facilities, and Internet access. Wright State University is a state supported university located in the Dayton metropolitan area, a high technology environment composed of several industrial, corporate and military research and development

facilities. Review for positions will begin December 1, 1990 and continue monthly until filled. Send letter of applications, resume, names of three references, and official copies of transcripts to: CSNET address-amcaulay@cs.wright.edu or Dr. Alastair D. McAulay, Chair, Department of Computer Science and Engineering, Wright State University, Dayton, OH 45435. An equal opportunity/affirmative action employer.

San Jose State University Electrical Engineering Department. Applications are invited for entry-level tenure-track faculty positions at the Assistant Professor rank. Positions are available in computer and multiprocessor design, microprocessor design, microprocessor application; analog and digital electronics, including CAD and VLSI; DSP architecture and application; circuits, systems and signal processing. Earned doctorate in Electrical Engineering is required. Positions are limited to U.S. citizens or permanent residents. Research, consulting and summer employment opportunities are available. The University is the oldest and one of the largest in the California State University System. It is located at the southern end of San Francisco Bay in the heart of Silicon Valley. Resume and names and addresses of three references should be submitted to Dr. Ray R. Chen, Chair, Department of Electrical Engineering, San Jose State University, San Jose, California, 95192-0084. San Jose State University is an equal opportunity/affirmative action/Title IX employer. Women and minorities are especially encouraged to apply.

University of Illinois at Chicago—Instructorships and Tenure-Track faculty positions in electrical engineering and computer science at both the junior and senior level are available. Rank and salary commensurate with qualifications. An earned Doctorate in EE or CS must be completed by date of appointment, but not for the instructorships. Demonstrated teaching and research abilities are highly desirable. For full consideration, please send resume, list of publications, and the names of at least three references by April 30, 1991, to Dr. Wai-Kai Chen, Head, Department of Electrical Engineering and Computer Science (M/C 154), University of Illinois at Chicago, P.O. Box 4348, Chicago, IL 60680. The University of Illinois is an Affirmative Action/Equal Opportunity Employer.

The Mechanical Engineering Department at Carnegie Mellon University invites applications for a tenure-track position at the Assistant Professor level Commencing September 1991 in the area of Robotics and Controls. This position is joint with the Robotics Institute at Carnegie Mellon. Applicants must have a Ph.D. in Mechanical Engineering (or closely related field). Duties include teaching undergraduate and graduate courses, and research. Appointments at a higher rank will be considered for qualified applicants having a proven record of grant support. Submit application, complete resume, and names of three references to Professor G.B. Sinclair, Mechanical Engineering Department, Carnegie Mellon University, Schenley Park, Pittsburgh, PA 15213-3890. Closing date for applications is February 15, 1991. Carnegie Mellon University is an affirmative action/equal opportunity employer.

Postgraduate Researcher. Two-year project for the development of dynamic neural networks that embody biological algorithms for pattern formation and recognition. Emphasis will be placed on use of chaotic dynamics. Experience in digital circuit design and fabrication, "C" and UNIX for solving sets of coupled nonlinear differential equations using numerical techniques, and MacIntosh II system. Beginning date 1/1/91. Salary: $2176/month. Credentials: Recent Ph.D. in Electrical Engineering and Computer Science. Send applications by 11/30/90 to Dr. Walter J. Freeman, 129 LSA, Division of Neurobiology, Department of Molecular and Cell Biology, University of California, Berkeley, CA 94720 USA, (415) 642-4220, FAX (415) 643-6791. The University of California is an affirmative action/equal opportunity employer.

Clemson University. Department of Electrical and Computer Engineering. The Department of Electrical and Computer Engineering at Clemson University invites applications for tenure/tenure-track positions, primarily at the assistant professor level. A Ph.D. is required. Candidates with research interests in one of the following areas are sought: communications and digital signal processing; networks and distributed computing; quantitative analysis of computer architectures; electromagnetic analysis of active devices (microwave, millimeter wave, or electro-optic); and multidisciplinary applications in power systems (e.g. power and artificial intelligence; power and computer communications). A successful candidate must exhibit exceptional potential for research and teaching. Clemson University's College of Engineering was listed as one of the United States' "up-and-coming" engineering graduate programs in the March 19, 1990, issue of U.S. News and World Report. The ECE Department comprises thirty-six full-time faculty, approximately 700 undergraduate students, and 140 graduate students. It offers B.S., M.S., and Ph.D. degrees in both electrical engineering and computer engineering. Facilities and/ or groups bearing on the areas indicated above include the Clemson University Electric Power Research Association (CUEPRA); a microcircuits reliability research group with a class 100 clean room; automated microwave measurement facilities to 26 GHz; an image processing laboratory; a Center for Computer Communication Systems. Resumes, supported with a list of references, should be sent to L. Wilson Pearson, Head; Department of Electrical and Computer Engineering; 102 Riggs Hall; Clemson University; Clemson, SC 29634-0915. Initial screening of applicants will begin January 15, 1991 and continue until positions are filled. Clemson University is an Equal Opportunity/Affirmative Action Employer.

University of California, Berkeley Institute of Transportation Studies. Research Position Available. The Institute of Transportation Studies, and Organized research unit of the University of California at Berkeley, has a large multi-disciplinary research program, the Program on Advanced Technology for the Highway (PATH), which covers a broad range of transportation related topics. The Institute is filling an Associate Specialist position for an electrical engineer for the program. The successful candidate will be responsible to: Conduct research, evaluation, design and perform experiments on advanced road vehicle lateral control techniques, particularly on the sensing/reference system. Develop a sensing reference/system using an electromagnetic sensing technique. Collaborate in the theoretical analysis of magnetic fields, signal processing, information coding and decoding techniques. Conduct studies on the reliability and safety related issues to explore possible approaches for maximizing safety of the lateral control system. Work together with other university researchers and engineers from automobile companies in developing the lateral control system. Supervise the work of graduate students. Qualification: This position requires knowledge of the worldwide state of the art in technologies for automatic lateral guidance of road vehicles, as well as expertise in the development and specification of electromagnetic sensing technologies. This applicant should also demonstrate analytical and experimental expertise in engineering of systems for maximum safety. This expertise should include principles of Fail-Safe and fault-tolerant system design, as well as use of Failure Mode Effects and Criticality Analysis. This position requires a minimum of a master's degree in Electrical Engineering plus at least four years of related experience in this field. Salary: Commensurate with qualification; to be determined at the time of appointment. The salary range is $36,648—$44,172 per year. Job site is in Richmond, California. Applicants should send curriculum vitae and names of three references to Director, Institute of Transportation Studies, 109 McLaughlin Hall, University of California, Berkeley, CA 94720. [tel. (415) 642-3585]. Deadline: November 30, 1990 or 30 days from publication data, whichever is later. The University of California is an Equal Opportunity, Affirmative Action Employer.

The University of Alabama (Tuscaloosa). A tenure-track position exists in the Department of Electrical Engineering for an assistant professor. Special departmental needs are in the areas of power systems, modern digital control, communications, optics/lasers and computer systems. However, outstanding applicants from other specializations will also be considered. Tuscaloosa, located in the rolling hills of West Alabama with a metropolitan area population of 150,000, is a one-hour drive west of Birmingham and three hours from Huntsville, Alabama where many NASA and DOD research facilities are located. Duties include both teaching and research activities. The faculty member is expected to develop an externally funded research program which will involve graduate students. Applicants must have an earned doctorate in Electrical or Computer Engineering with U.S. citizenship or permanent resident status preferred. Salary is commensurate with qualifications. Send a resume to Dr. Jon G. Bredeson, Head, Department of Electrical Engineering, The University of Alabama, Box 870286, Tuscaloosa, Alabama 35487-0286. The Search Committee will begin considering applications January 7, 1991, and will continue until the position is filled. The University of Alabama is an Equal Opportunity/Affirmative Action Employer.

University of Southern California. The Department of Electrical Engineering-Systems at the University of Southern California has faculty positions available at the Assistant, Associate for Full Professor level in the following areas: Communications Science (optical communications with an experimental emphasis, digital signal processing), and Signal and Image Processing (hardware for signal processing-analog, digital). Computer Engineering within the Electrical Engineering-Systems department is expanding, and looking to fill positions in the following areas: VLSI/CAD, networks (optical type), and architecture with an emphasis on hardware. Additionally, we are looking for a full-time instructor (M.A. only required) to support the Computer Science/Computer Engineering undergraduate degree program. For all openings, please send a resume and the names of at least three academic reference to Jerry M. Mendel, Chairman, Department of Electrical Engineering-Systems, University of Southern California, Los Angeles, CA 90089-0781. USC is an equal opportunity/affirmative action employer.

Brigham Young University-Computer Science Department. Applications are invited for an Assistant Professor position in Communications/Networking or Software Engineering beginning September 1991. Candidates must have a Ph.D. in Computer Science Applicants should send a curriculum vita to E. Daniel Johnson, 3362 TMCB, Brigham Young University, Provo, UT 84602.

University of Nebraska-Lincoln, Department of Electrical Engineering. The department seeks qualified candidates for a tenure-track faculty position in the area of control systems. Experience and interest in large scale, nonlinear, stochastic, adaptive or optimal control systems are desired. The department also anticipates other position openings and opportunities for joint appointments with the University's Research Centers in other areas. Applicants with expertise and interests in other areas of electrical engineering are also encouraged to apply. Rank and salary will be commensurate with qualifications. However, applications will be grouped and reviewed by academic rank, with hiring preference given first to the assistant professor level, then to associate and full professor level. Applicants must be U.S. citizens or hold permanent U.S. residency, hold an earned doctorate or anticipate receipt of it within six months of initial appointment, should have a strong interest in teaching at all levels and in developing research activity supportive of the department's growing graduate programs. Minority and women candidates are strongly encouraged to apply. Send a letter of application, resume, and a list of three references with addresses and telephone numbers by February 1, 1991 (or until suitable candidate is found thereafter) to: Dr. R.J. Soukup, Chair, Department of Electrical Engineering, University of Nebraska-Lincoln, 212N, WSEC, Lincoln, Nebraska 68588-0511. Affirmative Action/Equal Opportunity Employer.

Electrical Engineering: The Department of Electrical and Computer Engineering at the University of the Pacific is accepting applications for a tenure-track position at the Assistant or Associate Professor level. A Ph.D. is preferred, although an MS with significant industrial experience will be considered. Undergraduate education is the primary responsibility; curriculum development, advising, MS-level teaching and clinic supervision, and scholarly activity/research are also expected. UOP is a private, comprehensive university with a total enrollment of approximately 3800 students. Send resume to: Dr. George Schroeder, Electrical and Computer

Engineering, University of the Pacific, Stockton, CA 95211. UOP is an equal opportunity, affirmative action employer.

University of Maryland Baltimore County Dept. of Electrical Engineering anticipates several openings for tenure-track positions. The rapidly expanding program is part of the Electrical Engineering Department of the University of Maryland system. We are seeking candidates in the areas of digital signal processing and optical communications to strengthen ongoing efforts in image processing, pattern recognition, modulation and coding, and signal processing and to complement our existing experimental photonics program. Candidates should expect to teach undergraduate/graduate electrical engineering courses and conduct research in their areas of specialization. Rank and salary commensurate with qualifications. Send resume, list of three reference and a statement of research interests by April 1, 1991 to Dr. Gary M. Carter, Chairman Faculty Search Committee, Department of Electrical Engineering, University of Maryland Baltimore County, Baltimore, MD 21228-5398. UMBC is an EO/AA employer.

The University of Texas at Austin, Electrical and Computer Engineering Department is accepting applications for tenure-track faculty positions at the assistant professor level. Qualifications include an outstanding academic record, significant achievement in original research, sincere interest in teaching, and a doctorate in electrical or computer engineering/ science. Duties will include teaching undergraduate and graduate courses. Interested applicants are invited to send resumes which detail their past professional accomplishments, and which include the names and addresses of three references, to Dr. Mario J. Gonzalez, Chairman, Department of Electrical and Computer Engineering, The University of Texas, Austin, Austin, Texas 78712-1084, an Equal Opportunity/Affirmative Action Employer.

Faculty Positions in Electrical and Computer Engineering, State University of New York at Buffalo. Tenure track faculty positions are anticipated at all levels beginning August, 1991, with emphasis on Semiconductor Materials, Modelling of Submicron Devices, Photonics, Computers and Communications Engineering. Applicants must have an earned doctorate, with teaching and research interests in one or more of the following areas: device fabrication; plasma processing; modelling and design for VLSI; microwave semiconductors; semiconductor growth by Molecular Beam Epitaxy; photonics; communications; expert systems; computer architecture; data structures; parallel processing; and artificial intelligence. These positions will involve undergraduate and graduate course development and teaching, and the establishment of externally supported research programs. The Department has 31 faculty, 200 full-time graduate students, and 420 undergraduate students at the Junior and Senior level. Major facilities exist in semiconductors, superconductors, lasers, power and plasmas, image processing, VLSI, microwave, and computers. Centers of excellence are established in Superconductivity, Electronic and Electro-optic Materials and Power Conditioning. Applicants should supply a resume with names and addresses of three or more individuals for letters of reference. Applications may be sent to Professor W.A. Anderson, State University of New York at Buffalo, Department of Electrical and Computer Engineering, 201 Bell Hall, Buffalo, NY 14260. SUNY at Buffalo is an equal opportunity/affirmative action employer.

Graduate Research Assistant or Research Associate positions in optoelectronics. Must have hands-on knowledge of III-V compound semiconductor technology. Experience in remote PECVD a big plus. Send resume to: Dr. V. Malhotra, Department of Electrical Engineering, University of Hawaii at Manoa, 2540 Dole Street, Holmes Hall 450, Honolulu, Hawaii 96822. Fax No: (808) 956-3427.

Carnegie Mellon University. Graduate Study in Engineering and Public Policy (EPP): The EPP Graduate Program leads to a research-based Ph.D. specializing in policy issues in areas such as: telecommunication, computer and other information technologies; design and application of conventional and AI-based computer systems for policy analysis and decision support; mathematical modeling of energy and environmental systems; technical and economic issues of peace and international security; manufacturing and industrial policy; and risk analysis. Applicants must hold a Bachelor's Degree in engineering, physical sciences, or mathematics. Education or experience beyond the Bachelor's Degree is very desirable. Contact Dr. Indira Nair, Engineering and Public Policy (06), Carnegie Mellon University, Pittsburgh, PA 15213.

Faculty Position in Medical Imaging. The Curriculum in Biomedical Engineering and Mathematics (BMME) and the Department of Radiology at the University of North Carolina at Chapel Hill invite applications for a tenured-track faculty position at the Assistant/Associate Professor level beginning in early 1991. Candidates should have a Ph.D. degree in engineering, physics, applied mathematics, or a related area and be experienced in medical imaging research. Preference will be given to candidates who specialize in the areas of X-ray, MRI and/or Ultrasound imaging. The successful candidate should have experience or demonstrated potential in securing external research funding. He/she is expected to participate in teaching in the graduate program of BMME and to advise graduate students in dissertation research. He/she will join another faculty member in BMME and a diverse group of scientists from the Departments of Radiology, Computer Science and Radiation Oncology who are actively pursuing different areas of medical imaging research. Send resumes to Carol L. Lucas, Ph.D., Professor and Acting Chair, Biomedical Engineering and Mathematics, CB #7575, 152 MacNider Hall, The University of North Carolina, Chapel Hill, NC 27599-7575 before October 1, 1990. The University of North Carolina is an Equal Opportunity/Affirmative Action employer.

Lafayette College: Two tenure-track Assistant Professor positions beginning August 1991, in the Electrical Engineering Department. Disciplines of interest are Microelectronics, Communications, and Digital Signal Processing. Requires PhD in Electrical Engineering and a strong commitment to undergraduate education. Lafayette College enrolls 2,000 students and is an independent, highly selective undergraduate institution having EAC/ ABET-accredited programs in four engineering disciplines. Women and minorities are encouraged to apply. Send resume, with three reference and statement of teaching and research interests, to Dr. William Hornfeck, Electrical Engineering Department, Lafayette College, Easton, PA 18042. An Equal Opportunity Employer.

Faculty Position Announcement in Electrical Engineering. The Department of Electrical Engineering, University of Hawaii at Monoa, invites applicants for tenure-track assistant and associate professor positions with specialization in any of the following three areas; (1) Computers: Knowledge of distributed computing and network architecture, multi-media data and knowledge-based systems, and intelligent multi-sensor systems; (2) Electrophysics: Electronic circuits, IC semiconductor devices, IC technology, Instrumentation, microwave engineering, and sensors (biosensors, optical, micromechanical and other); (3) Communications: Data networks. Duties: Teach EE undergraduate and graduate courses, serve on university and department committees, serve on graduate student committees, conduct research and scholarly activities, and perform related tasks as assigned. Minimum qualifications: Assistant Professor: Ph.D. degree or completion of all requirements for a doctorate in Electrical Engineering, demonstrated ability to teach, demonstrated scholarly achievement, ability to pursue and supervise research; strong commitment to both undergraduate and graduate teaching. Associate Professor: Ph.D. degree in electrical engineering; minimum of four years of full-time college or university teaching at the rank of assistant professor or equivalent, with evidence of increasing professional maturity; demonstrated scholarly achievement in comparison with peers active in the same field; demonstrated ability to plan and organize assigned activities including the supervision of work assignments when appropriate; ability to pursue and supervise research; strong commitment to both undergraduate and graduate teaching. Minimum annual salary: $50,364 (assistant professor) and $63,732 (associate professor). Salary negotiable dependent upon qualifications and experience. Send resume and three letters of reference by December 10, 1990 to Professor Shu Lin, Chairman, Department of Electrical Engineering, University of Hawaii at Manoa, 2540 Dole Street, Homes Hall 483, Honolulu, Hawaii 96822.

Electrical Engineering Professorial Positions. Professorial positions are available in Signal Processing, Computer Systems, Electronic Applications and Quality. Further information can be obtained from the Personnel Department, Queensland University of Technology, telephone 617 223 2906, facsimile 61 7 229 3193 or write to the Personnel Director QUT GPO Box 2434 Brisbane Queensland 4001 Australia. Applications close 30 November 1990.

E.E. Faculty Positions at Auburn University. E.E Department currently has openings for faculty with expertise in any of the following areas: computer engineering, VLSI design, electronic circuit design or power engineering. Applicants must be research oriented, have a Ph.D. and an electrical engineering background. Senior level appointments are available. Foreign national applicants must clearly indicate visa status. Auburn is Alabama's land-grant university with 22,000 students. The E.E. Department has 30 faculty and currently enrolls approximately 750 undergraduate and 120 graduate students. The annual research funding level is approximately $3 million. Interested persons may send resumes to Professor L.L. Grigsby, Chairman of Faculty Search Committee, Department of Electrical Engineering, Auburn University, AL 36849-5201. Minorities and women are encouraged to apply. Auburn University is an equal opportunity and affirmative action employer.

Western Michigan University, the Department of Electrical Engineering invites applications for an anticipated tenure-track faculty position at the Assistant/Associate/Full Professor level. Preferred applicants must have an earned PhD in Computer Engineering or the equivalent and specialize in computer engineering and design. Responsibilities include graduate and undergraduate teaching, curricular leadership, and research. Western Michigan University is located in Kalamazoo, Michigan and has approximately 26,000 students; it is one of the state's five graduate intensive universities and is designated a Carnegie Doctoral I university. The Department offers two EAC/ABET accredited undergraduate degrees (Computer Systems Engineering and Electrical Engineering) and a growing graduate program. We are looking for an experience computer engineering faculty member who enjoys teaching and would like to participate in building a design oriented graduate program in computer engineering. Please send a detailed resume, including a statement of citizenship, and names of three references to: Dr. Thomas F. Piatkowski, Chair, Department of Electrical Engineering, Western Michigan University, Kalamazoo MI 49008-5066 or piatkowski@gw.wmich.edu. Applications will be accepted until the position is filled. Western Michigan University is an affirmative action employer/equal opportunity institution.

University of Houston. The Department of Electrical Engineering invites applications for tenure-track positions in the areas of applied electromagnetics, biomedical engineering, communications, computer engineering, electronics and microelectronics. Openings are available at all ranks. Please send resumes to Dr. J.C. Wolfe, Department of Electrical Engineering, University of Houston, Houston, TX 77204-4793. An Equal Opportunity Employer.

Lehigh University, Chairperson, Department of Electrical and Computer Engineering. The College of Engineering and Applied Sciences at Lehigh University invites applications and nominations for the position of Chairperson of the Computer Science and Electrical Engineering (CSEE) Department. The Department has 26 full-time faculty, 350 undergraduates and 200 graduates (80 full-time) with an annual research budget of $3M. In addition, the CSEE Department awards annually about one-third of all engineering degrees at the undergraduate and graduate levels. The chairperson position is an endowed chair with a full professorship. A per-

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New military profile	206	207	208
Defense industry	209	210	211
Roundtable	212	213	214
Fuzzy logic	215	216	217
Selecting microcontrollers	218	219	220
Advanced DRAMs	221	222	223
Canon reinvents itself	224	225	226
Blue box	227	228	229
Niagara's 25-Hz generators	230	231	232
Japan's phones	233	234	235
Global manufacturing system	236	237	238
Paperless office	239	240	241
Newslog	242	243	244
Spinoffs	245	246	247
EEs' tools & toys	248	249	250

Did you find this material stimulating or thought-provoking?

Item	Yes	No
Spectral lines	251	252
Reflections	253	254
Forum	255	256
Books	257	258
Managing technology	259	260
Technically speaking	261	262

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University of Notre Dame—Chairperson, Department of Computer Science and Engineering. The University of Notre Dame invites applications for the Chair of the recently established Department of Computer Science and Engineering in the College of Engineering. This position is a unique opportunity to provide significant input in establishing direction for the initiation and growth of programs in this department. Persons with established records in education and scholarship who would welcome the challenge of developing a new department and its programs are encouraged to apply. The faculty of the department is expected to determine the curricula leading to graduate and undergraduate degrees in computer science and in computer engineering. The Department of Computer Science and Engineering has twelve tenure-track faculty positions. The Department of Electrical Engineering and its present graduate and undergraduate options of emphasis in computer engineering are expected to provide the foundation for the programs in the new department. It is anticipated the Department of Computer Science and Engineering will have close cooperative ties with the Department of Electrical Engineering, Department of Mathematics, and other academic units. Qualified applicants are encourage to submit a resume and letter of interest to: Dr. Panos J. Antsaklis, Department of Electrical Engineering, University of Notre Dame, Notre Dame, IN 46556. For additional information, please contact the Dean's office at (219) 239-5534. The University of Notre Dame invites applications from all qualified persons without regard to sex, ethnic origin, religious preference or physical impairment.

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Facilities & CIM Control Engineer for manufacturing firm in central Ohio. Develop, design and implement state of the art control strategies in area of power, specifically medium, low, & high voltage power & lighting systems conforming to NEC, transformers, motors, motor control centers, grounding, short circuit and voltage drop studies, ground fault and overcurrent protection, as well as in the area of Computer Control & Instrumentation, specifically development of expert systems & application software for factory floor manufacturing & management systems utilizing CIM (Computer Integrated Manufacturing) & MAP (Manufacturing Automation Protocol); control logic for PLCs; CAD drawings; PID Loops & Instrumentation techniques in coffee extraction process. Prepare applications for expenditure & control of project budgets. Supervise installation & start-up, coordinating outside contractors & in-plant electricians. Must have M.S. in EE, (Control Systems) and 2 yrs. exp. in above duties or 2 yrs. as Elect. Engin. - Power Instrumentation & Control Systems. Prior exp. must include 1 yr. programming Allen Bradley & Texas Instruments Programmable Logic Controllers. Must have applied short-circuit analysis (thru educ. or exp.) & written programs in FORTAN, COBOL & PASCAL. (thru educ. or exp.) Two yrs. exp. must also include installing systems conforming to NEC, 1 yr. exp. using Computer Assisted Design techniques & 1 yr. exp. in coffee extraction process. Must have proof of legal authority to work permanently in U.S. Mon.-Fri., 8a.m.-5p.m.; $45,000/yr. Send resume in duplicate (no calls) to J. Davies, J.O. #1260436 OH Bureau of Employment Services, P.O. Box 1618, Columbus, OH 43216.

Manager, Project Management Development—Bachelor degree (or equivalent) in Control or Electrical Engineering, or in Computer Electronics and Electrical Engineering Technology and 8 years of experience as Electric Utilities Control Engineer or Manager, project management development; knowledge and experience in installing/maintaining/operating SCADA systems; computer fluency in communication mediums; duties include management of all SCADA projects and supervision of quality control and engineering activities; 40 hrs/wk; $45,000-$60,000 salary ("DOQ"). Contact Georgia Department of Labor at 1535 Atkinson Road, Lawrenceville, GA 30243, #GA 5441183.

Engineer, Control Systems. Supervise design and engineering for digital and analog electronic systems. Oversee generation of wiring diagrams, and design interconnecting cable systems to marshaling panels, local control panels, or field devices. Design of analog control signals to the Honeywell DCS system, and digital control signals as well as shut-down logic signals to the PLC system. Generate DCS, PLC and SCADA functional and detailed specifications. Utilize DBASE III Plus, Lotus and computer-aided instrument electrical system software. Reqs. a BS in Electronic/Electrical Engineering with a minimum of five years of supervisory-level employment in conceptual, basic and detail design engineering, scheduling, estimating, procurement, and start-up in instrumentation, control and SCADA systems. Exp. must include the specification, design and application engineering of algorithms for proper DCS interface and operation, P&ID development of DCS based control system strategies, and documentation of complex control loops, and must include application engineering for standard PLC systems. Specific knowledge of Honeywell TDC 3000 DCS is required, as well as the ability to develop the software configurations. Must be skilled in using DBASE III Plus and Lotus. Position based out of San Francisco, but subject to

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Electronics Engineers—Washington, DC/Maryland/Virginia. Engineering placement Leaders since 1973. Specializing In Product Development (Hardware & Software), Communications, Artificial Intelligence, Military Electronics, Computer Engineering and VLSI/ASIC. Direct resume to: JDG Associates Ltd., 1700 Research Blvd., Rockville, MD 20850 - (301) 340-2210.

Engineer, Electronics. Research on semiconductor device testing & circuit evaluation; radiation damage & laser effects on devices & circuits (including total dose effects & transient upset effects); perform reliability analysis & computer modeling of devices; provide computer software support (system maintenance, networking & developing X-window related & HP-IB based software). PhD. in EE + knowledge in device physics, Si & GaAs field effect transistors, radiation damage effect on devices & circuits, modeling & characterization of submicron FET transistors (hetero-junction based on GaAs, unipolar device [MOSFET, MESFET, MODFET], microwave characterization of GaAs devices up to 20GHz), quantum mechanics, solid state electronics & circuit design, processing of Si & GaAs, deep-level characterization in semi-insulating material & devices, numerical analysis, simulation software (SPICE, PISCES, MINIMOS, SUPREM), FORTRAN, C PASCAL, BASIC w/i UNIX, VAX/VMS, HPIB, UNIX shell & window systems req'd. $3625.00/mo. Job site/interview: Sunnyvale, CA. Send ad with resume to Job #DC-16743, P.O. Box 9560, Sacramento, CA 95823-0560,no later than 12/1/90.

Scientific Programmer—Position available to research and design mathematical algorithms that perform large-scale electrical utility network steady state contingency analysis on real-time energy management computer systems. Will use FORTRAN to code algorithms and integrate into large, multi-main frame computer system. Must have masters degree in electrical engineering, with research in steady state contingency analysis functions of large-scale power systems and at least four years experience with either an electric utility or vendor of power systems, as a scientific programmer developing in FORTRAN contingency analysis software on large-scale real-time power systems. Must be a U.S. citizen or permanent resident. Salary $3535/month. Send resume to: S. Springmeyer #0-205, Minnesota Department of Jobs & Training, 390 N. Robert St., Room 124, St. Paul, MN 55101. Affirmative Action Employer.

Engineering Physicist II. As Assistant Leader of the Electronic Group assigned to the development and construction of a very large high-energy physics detector, this position is responsible for the specification, procurement, inspection, installation and commissioning of all cable, connectors and associated electronics which will provide power, control and data transmission to the detector and between the detector and experiment data acquisition systems. Use of a P.C. for access to a data base of cable specifications, inventory and connection locations is required. This is a research position of 40 hours per week (8:30 a.m.—5:00 p.m.) and carries a salary of $45,400 p.a. As a minimum, applicants should possess a B.S. in Physics and demonstrate five years as a project leader in cable system development/installation/commissioning. Resumes should be sent to: Illinois Department of Employment Security, 401 South State Street—3 South, Chicago. Illinois 60605, Attention: L. Donegan, Reference #1780-D, An Employer Paid Ad.

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Engineer, Electro/ Optical: Support on-going contracts; dev. code & techniques for specific products; dev. software & algorithm for NDE technologies; R&D new techniques for advanced NDE inspection systems; dev. data analysis & code for X-ray computed tomography & digital radiography systems. PhD in EE + knowledge in signal & image processing & reconstruction algorithms; numerical techniques for inverse problems & applications to computerized tomography req'd. Must also know C. Fortran on VAX/VMS & workstations on UNIX. $4043/mo. 40 hrs./wk. Job site/interview: Sunnyvale, CA. Send ad with resume to Job # BLW18265, P.O. Box 9560, Sacramento, CA 95823-0560 no later than November 15, 1990.

Help Wanted: System Software Engineer, Data Access Business Unit Testing Group. By December 1st please send resume to: Employment Security Department, ES Division, ATT: Job # 230081, Olympia, Washington 98504. Job Description: Designs, implements and tests complex and high level systems software for micro computers. Works with other engineers to coordinate and implement testing and debugging of BASIC language products utilizing MS-DOS and OS/2 and LAN Man operating systems, and Basic, "C" and 8086 Assembler Series languages. Responsible for testing the Basic Compiler, debugger and development environment and establishing, analyzing and improving quality control procedures for language products. Assumes major project responsibility including: 1) requirements and analysis of project specifications; 2) product design; and 3) implementation schedules. Requirements: B.A. or B.S. In Electrical Engineering, Computer Science, Mathematics or Physics. Six months work experience designing and testing compilers, debuggers and development tools and establishing and analyzing quality control procedures for language products; and in computer design or programming utilizing MS-DOS, multitasking and networking operating systems and Basic, "C" and 8086 assembler series languages. Must have proof of legal authority to work in the United States. Job location: Redmond, Washington. Salary Range: $29,000-34,000 per annum, depending on experience. 40 hours per week, flex time. EOE.

Instrument/Electrical Maintenance Engineer II. Will plan and direct the preventive maintenance program to insure the timely upkeep of all electrical, electronic and pneumatic equipment in the plant. Will conduct infrared scanning, transformer oil testing, calibration of high voltage relays and medium voltage circuit breakers, trip testing of inverters, load checks on back-up battery banks, visual and aural inspection of motor control centers, motors and transformers, and annual calibration of shut-down switches on all compressors and turbines. Will direct and assist technicians in locating the cause of equipment failure and assist as necessary to effect repairs. Will perform engineering design work for new installations or improvements to existing facilities. Will prepare equipment specifications and provide assistance to Purchasing Department in securing required equipment and materials. Requirements: B.S. In Electrical Engineering. Two years experience as Instrument/Electrical Maintenance Engineer I or equivalent. Two years experience in maintenance, calibration and repair of gas chromatrograph (all experience may be obtained concurrently). $38,000/year; 8 A.M. to 5:00 P.M. (hours may vary upon demand); 40 Hr/ week. Contact LA Office of Employment Security, Job order 472735, 1028 Enterprise Blvd., Lake Charles, LA 70602.

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Engineering, 3 yrs in position offered or 3 yrs in field of electrical engineering which must include at least 2 yrs research experience in development/analysis of LAN, MAN or broadband network technology and experience in design/analysis of computer communications networks and experience in design/analysis of voice/data/video services. Salary: $4500/mo. Job Site: San Ramon, CA. Send this ad and your resume to Job #CC 18536, P.O. Box 9560, Sacramento, CA 95823-0560, no later than November 30, 1990.

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'Peace dividend' means job losses

If Pentagon funds are reduced by 10 percent each year, compounded through 1996, a maximum reduction in demand for engineers would occur in 1995 when 44 000 engineers would be displaced. Electrical engineers would compose more than one-third of the total.

This information from unpublished National Science Foundation (NSF) data was presented by Robert A. Rivers, a member of the IEEE-USA Manpower Commission, to those attending the IEEE Professional Activities Council for Engineers conference in Phoenix, Ariz., in September.

The NSF data showed defense-related engineers hold 32 percent of the jobs in communications work; 43 percent of those in aircraft, parts, and guided missiles; and 28 percent of those in measuring and control instruments.

One of the news releases at the meeting showed that U.S. expenditures for national security are about 5 percent of the gross national product. Therefore if the economy grows at a 2.5 percent annual clip, defense cuts could be mitigated [THE INSTITUTE, November, p. 8].

Japan's speedy supercomputers

The US $24 million Model 44, the top of the line of NEC Corp.'s new SEX-3 series supercomputers, is rated at 22 billion floating-point operations per second (Gflops). The US $11 million low-end Model 14 is rated at 5.5 Gflops. NEC began shipping the supercomputers in June.

In comparison, a high-end Cray Y-MP8, to be installed at Tohoku University, is rated at a peak of 2.7 Gflops. It will rent for 89 million yen (US $0.64 million) per month.

Fujitsu Ltd.'s two new models—the VP2200/40 and the VP2400/40—have peak processing speeds of 2 and 5 Gflops, respectively, and will rent for 79 million and 103 million yen (US $0.56 million and $0.74 million) per month. They will be available in September 1991 [THE INSTITUTE, November, p. 1].

Changes in IEEE insurance plan

The IEEE Executive Committee has approved a series of changes in insurance benefits:

- Maximum insurance benefit under the IEEE In-Hospital Plan will be increased to US $300 per day for members and their dependents.
- A credit equal to 30 percent of the annual premium for the 1990–91 policy year will be given to all members insured in the Disability Income Plan as of Oct. 31, 1989.
- The base premium rates of the Guaranteed Acceptance Medical Plan and the Major Medical Plan are being hiked 20 and 10 percent, respectively, as of Nov. 1, 1990.
- The maximum benefit per illness or injury under the Guaranteed Acceptance Plan and the Major Medical Expense Plan will be increased to US $35 000 for claims beginning on or after Oct. 1, 1990.

IEEE Fellow nominees sought

Members are invited to submit nominations of those they would like to be elected to the Fellow grade. To qualify for Fellow grade, candidates must be Senior Members and have been members for at least five years before the one in which the election is to take place. However, the five-year membership requirement may be waived for a candidate in professional practice, and so qualified as a Senior Member, in a geographical area where it was difficult to become a member previously. [THE INSTITUTE, November, p. 8].

- The maximum room and board benefit under the Comprehensive Healthcare Plan is being doubled from US $400 to US $800 per day, effective Nov. 1, 1990 [THE INSTITUTE, November, p. 2].

COMING IN SPECTRUM

High-tech layoffs. For the last couple of years, there have been an unsettlingly large number of layoffs in high-technology industries. What does this mean for new graduates and veteran engineers, job stability, and career advancement?

Environment vs. electric power. In 1986 and 1987, Federal regulations governing the relicensing of hydroelectric power plants changed to accommodate environmental needs, including fish migrations—and that may discommode some of the 300 U.S. hydroelectric plants due for relicensing before the year 2000.

Electronics and the car of '91. Many new models boast electronically controlled automatic transmissions and suspensions. The Acura NSX, moreover, has an electronically controlled variable valve timing system and a direct ignition system with ignition coils for each spark plug. A similar ignition system is on some Saab cars.

Japanese robots. When a group of leading U.S. roboticists toured Japanese laboratories recently with an eye to space applications, they were impressed and on occasion awed by what they saw—for instance, a whole new class of serpent-like arms.

Parallelism in compilers. While parallelism has been present in one form or another in the the earliest computers, over the past decade it has played an increasing role in computer architectures. More especially, applications are evolving for computer compilers.

Whistleblower survivors. Not all engineers who openly disagree with their employers about the safety of a product or expose unscrupulous practices lose out. Three engineers who quit General Electric in the 1970s because they mistrusted existing nuclear reactor technology have since formed one of the most successful nuclear safety consulting firms in the United States.

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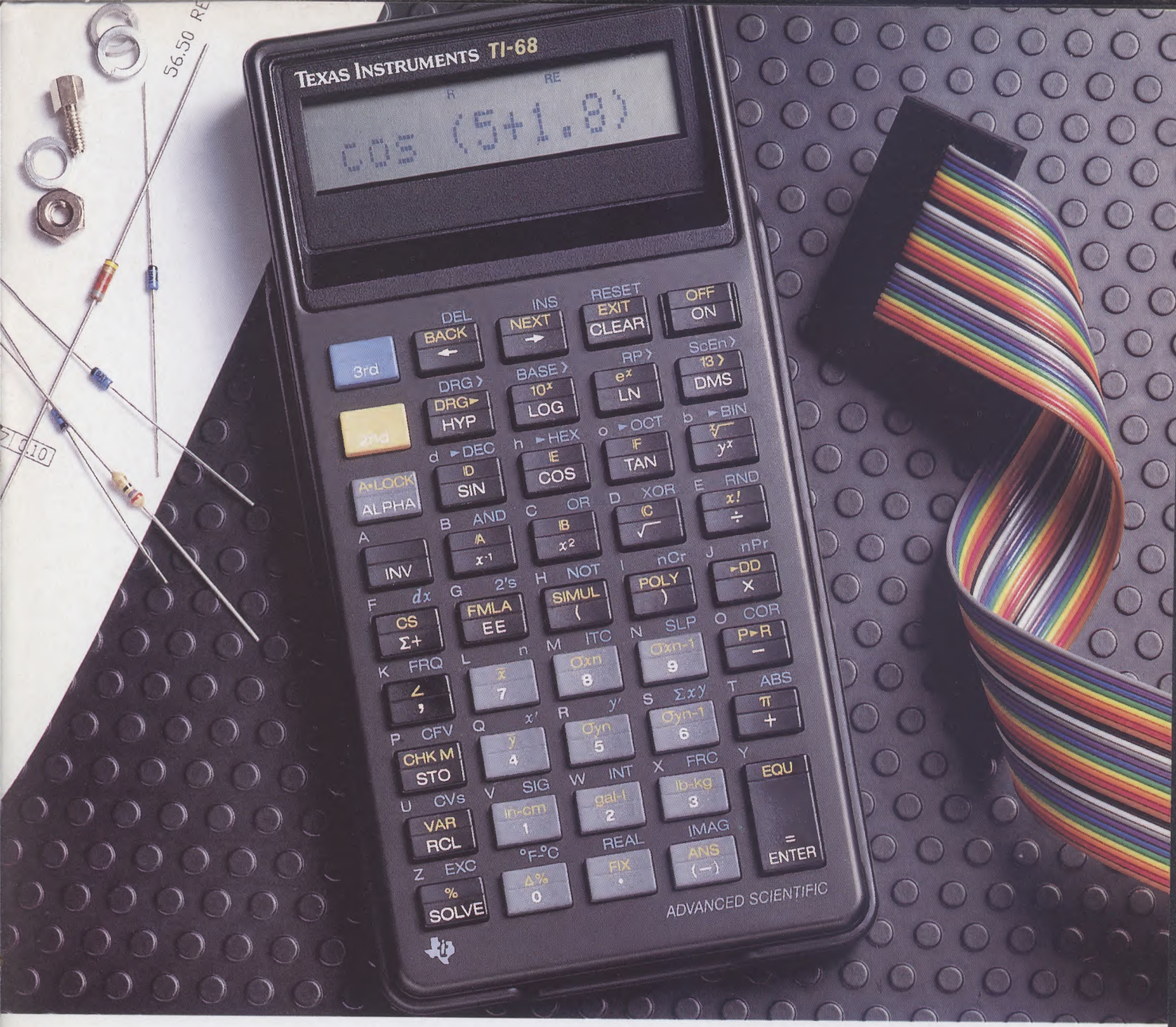
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RS#	Advertiser	Page #
23	Addison-Wesley Publishing	18E
30	Arizona State University	142
8	CSPI	15
5	Data Delay Devices	27
21	Dialog	18 I
2	DSP Development	cover 4
19	Hewlett-Packard Calculators	18K
24	Jandel Scientific	27
10	Lanier	23
9	Mathsoft	25
11	Maxwell Labs	12
20	Mensa	132
4	Mita Press	13
12	National Instruments	26
22	Netherland Foreign Investments	18G
6	Pearson Electronics	8
16	Penstock	12
3	RLM Research	8
1	Signal Technology	cover 2
31	Southeastern Center for Electrical Engineering Education	128 I
18	Systems Control Technology	18F
7	Teledyne Solid State	7
17	Texas Instruments Calculators	cover 3



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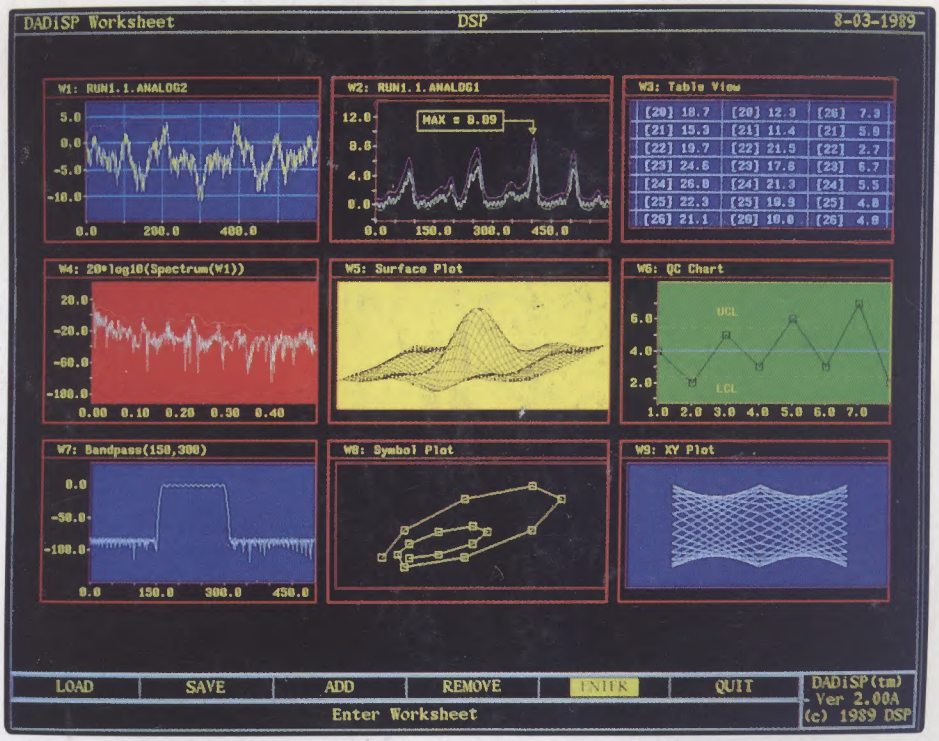
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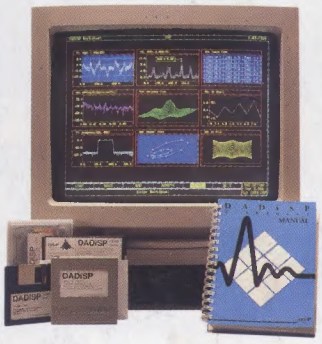
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